New MEGA POWER DUAL™ IGBT Module
with Advanced 1200V CSTBT Chip

Junji Yamada*, Yoshiharu Yu*,
John F. Donlon**, Eric R. Motto**

* Power Device Division, Mitsubishi Electric Corporation, Fukuoka, Japan
** Powerex Incorporated, Youngwood, Pennsylvania, USA

Abstract - **A new 1400A/1200V MEGA POWER DUAL™ IGBT module has been developed for high power industrial applications. The new module incorporates the latest advances in chip technology to produce a device with the rugged safe operating area and low losses required in high power industrial applications. The new power chip is based on an optimized wide cell pitch Carrier Stored Trench Bipolar Transistor (CSTBT). The module features an optimized high current dual (half bridge) package with low parasitic inductance and integrated features designed to allow simplified assembly of high power inverters.**

I. INTRODUCTION

The use of IGBT modules in megawatt class industrial inverters has required a rethinking of basic power structure design. The designer is faced with several fundamental challenges. The first is maintaining the low inductance necessary to control transient voltages while the physical size and length of the main bus interconnects increase. The solution to this problem usually involves a general shrinking of the power structure. This shrinking gives rise to a second problem, which is how to remove thousands of watts of losses from a relatively small heat sink area. In addition, the weight and intricacy of the laminated buswork and thermal system in these inverters often results in a complex assembly that is difficult and expensive to manufacture. The MEGA POWER DUAL^{TM} IGBT module presented in this paper utilizes advanced chip technology combined with a new package concept to help alleviate these problems.

II. NEW 1200V CSTBT CHIP

Fig. 1 shows an equivalent circuit model for an ideal IGBT in its on state. This circuit shows that the on-state voltage ($V_{CE(sat)}$) of an IGBT can be thought of as the sum of the forward voltage of a PIN diode and the $R_{DS(ON)}$ drop of a MOSFET. The $R_{DS(ON)}$ of the MOSFET portion of Fig. 1 can be decreased by increasing the total channel width per unit chip area. High-density trench gate surface structures have been developed to provide a substantial increase in channel width [2][4]. At the same time the trench gate structure eliminates the parasitic JFET resistance associated with the MOSFET. As a result, the largest component of on-state voltage in state-of-the-art trench gate IGBT devices can be linked to the forward voltage drop of the PIN diode portion of

Fig. 1.

Normally a PIN diode has a symmetrical excess carrier distribution in the n- region as shown by curve A in Fig. 2. Curve B shows that the excess carrier distribution in a conventional trench gate IGBT deviates from the ideal case by steadily decreasing as it approaches the emitter side of the device. This non-ideal behavior becomes even more pronounced in devices with high blocking voltage ratings. The decreased carrier concentration near the emitter side effectively increases the resistance of the PIN diode which results in an increase in on-state voltage ($V_{CE(sat)}$). To improve the carrier concentration at the emitter side a new chip design called Carrier Stored Trench Bipolar Transistor (CSTBT) has
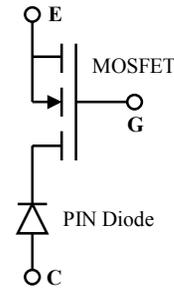

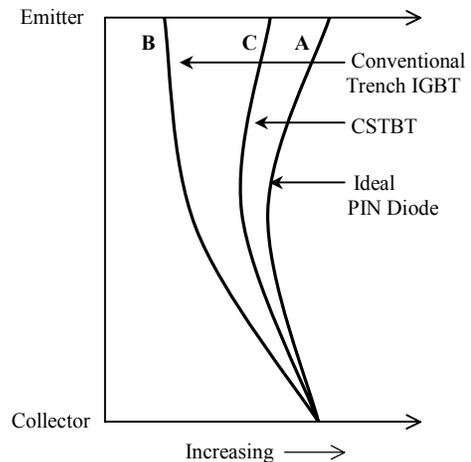Fig. 1 On-State Model of IGBT

Fig. 2 Excess Carrier Distribution in the n- Layer
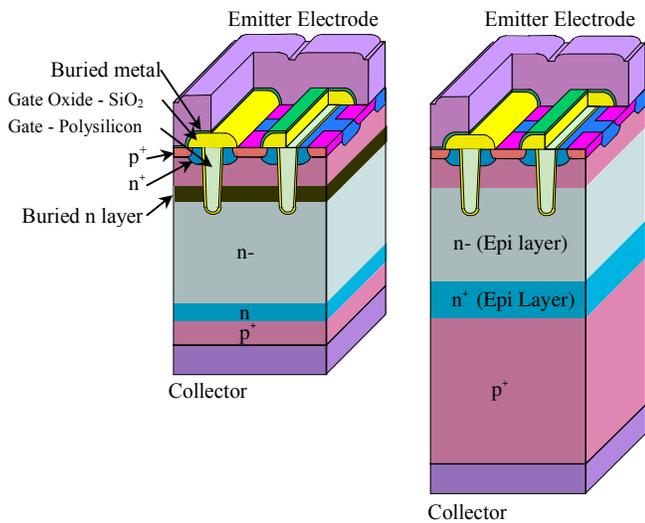
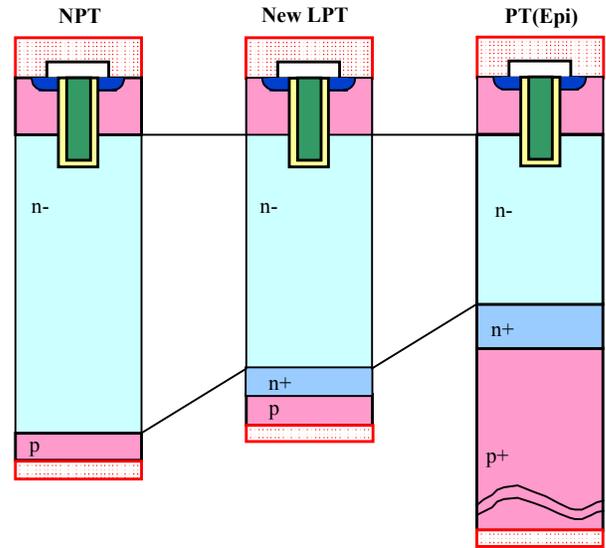Fig. 3a New CSTBT Chip   Fig. 3b Conventional Trench Gate IGBT

Fig. 4 Comparison of IGBT Vertical Structure

been developed. The CSTBT is fabricated with an additional n type buried layer.   The buried layer provides "stored" carriers to produce the modified carrier distribution shown in curve C of Fig. 2. The resulting carrier distribution is closer to the ideal case and produces increased conductivity in the n-layer. The result is a substantial reduction in the on-state voltage of the device. Fig. 3a and 3b show the cell structure of a conventional high cell density trench gate IGBT compared to the CSTBT. The key difference is the addition of the buried n layer to provide increased carrier concentration near the emitter side of the device.

In addition to the buried n layer, the new CSTBT chip utilizes an optimized vertical structure based on Mitsubishi's Light Punch-Through (LPT) technology.   A schematic comparison of conventional NPT, Epitaxial PT and LPT chips

is shown in Fig. 4.   The key to the LPT structure is an optimized n- drift region that it is thin enough to provide low $V_{CE(SAT)}$ while maintaining a robust switching SOA.   An n buffer layer is utilized to secure a sufficiently high breakdown voltage and low leakage current in the presence of the optimally thin n- drift region. The thickness of the n- drift layer is selected so that the depletion region extends to the collector when rated voltage is applied in the off state. However, at normal operating voltages the depletion region does not reach the buffer layer giving an operation characteristic similar to conventional NPT designs. Another feature of the LPT structure is optimized n+ buffer and p collector layers that provide controlled carrier concentration in the n- region during conduction. The result is efficient switching characteristics without the need for carrier lifetime
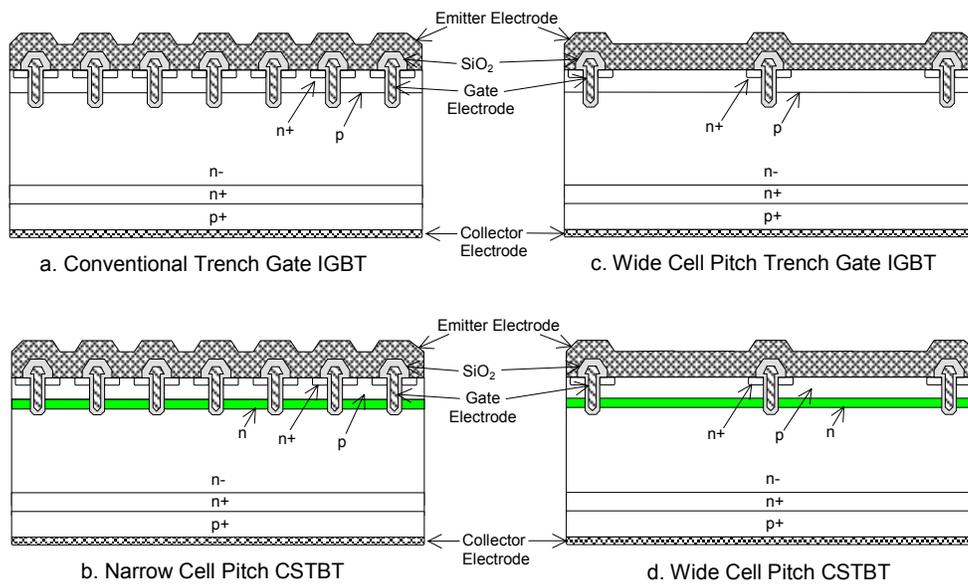

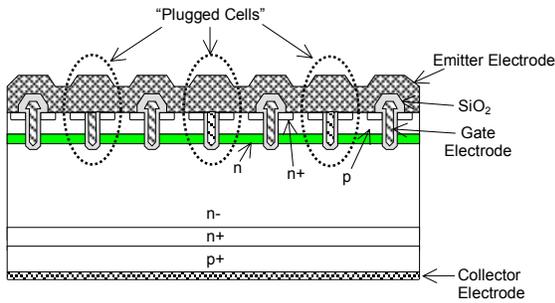Fig. 5 IGBT Chip Structure Comparison
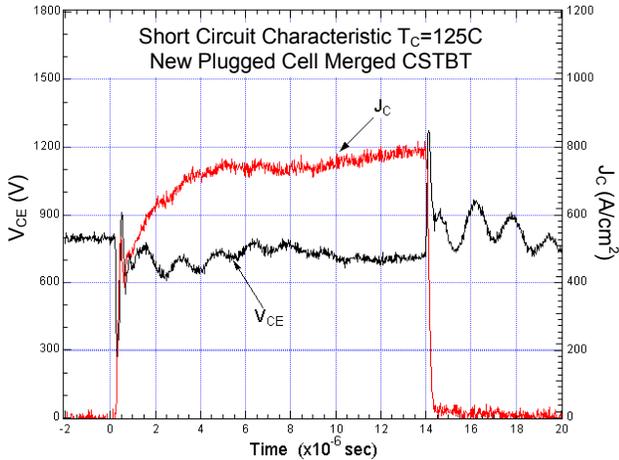
Fig. 6   Plugged Cell Merged CSTBT

Fig. 7   Short-Circuit Waveforms

control processing. The new CSTBT chips are fabricated from low cost n-type single crystal (non-epitaxial) wafer material.

Fig. 5a shows a conventional high cell density trench gate IGBT. The high cell density helps to reduce $V_{CE(SAT)}$ by making the $R_{DS(ON)}$ of the MOSFET part of the device very low. Unfortunately, the MOSFET part of this structure also permits very high short-circuit currents which degrades the short-circuit withstanding capability of the device. Under low impedance short-circuit conditions, the current becomes very high before the device desaturates and limits the current. The self-limited current of the IGBT is often called the short-circuit saturation current. The short-circuit saturation current for the conventional narrow pitch trench gate IGBT with V_{GE}=15V is more than fifteen times the nominal rated current of the device. This high short-circuit saturation current limits short-circuit withstanding capability of the chip alone to about 5μs. To recover the short-circuit withstanding capability required for many industrial applications, it is necessary to add an additional current limiting circuit to reduce the gate voltage under short-circuit conditions [2]. Unfortunately this increases the complexity of the device. Obviously, it is desirable to have a chip with a lower short-circuit saturation current so that this additional current limiting circuit would not be required.

The short-circuit saturation current of an IGBT is primarily controlled by the characteristics of the MOSFET part of the device. One effective way to reduce the short-circuit saturation current and improve short-circuit ruggedness is to reduce the total channel width of the MOSFET part of the IGBT structure. This can be accomplished by utilizing a wider cell pitch structure as shown in Fig. 5c. Unfortunately, reducing the channel width of the conventional trench gate IGBT increases the $R_{DS(ON)}$ of the MOSFET portion of the device resulting in an increased $V_{CE(sat)}$.

The CSTBT chip structure described above can be used to mitigate the undesirable increase of on-state voltage caused by a wider cell pitch design. The structure of the wide cell pitch CSTBT is shown in Fig. 5d. By selecting appropriate trench spacing and depth the series resistance and performance of the MOS and diode regions can be optimized to provide low on-state voltage while maintaining low short-circuit saturation current [4]. The short-circuit saturation current can be adjusted to provide short-circuit withstanding capability of 20μs eliminating the need for additional limiting circuits. At the same time, using the CSTBT structure increases the conductivity in the drift region to produce a low on-state voltage.

Selection of the optimal cell pitch allows the device to be tailored for the most desirable trade-off between short-circuit saturation current and $V_{CE(SAT)}$. For applications that do not require as much short-circuit withstanding capability, a narrow cell pitch can be used to give a lower $V_{CE(SAT)}$. A wider cell pitch can be useful for maintaining short-circuit ruggedness in higher voltage devices. To provide process flexibility with a minimum number of mask changes a novel structure called Plugged Cell Merged (PCM) CSTBT was developed. This structure is illustrated in Fig. 6. With this structure the cell pitch is adjusted by "plugging" some portion of the cells in a conventional high cell density device. This process allows the cell density to be optimized by changing only two masks.

Table 1 Comparison 100A, 1200V IGBT			
	3rd Generation	4th Generation	New CSTBT
Family Name	H-Series	F-Series	NF-Series
Base Wafer Material	Epitaxial	Epitaxial	Float Zone
Surface Pattern	3μm Planar	1μm Trench	1μm Trench PCM
Vertical Design	PT	PT	LPT
$V_{CE(sat)}$ @ $I_{C(rated)}$	2.5V	1.9V	1.9V
SWSOA	Over 300A	Over 400A	Over 400A
C_{ies}	9.6nF	24.3nF	12.8nF
Short-Circuit Current	600A	1500A (Without RTC)	500A
Short-Circuit Withstanding $t_{W(crit)}$	20μs	5μs (Without RTC)	20μs

The polysilicon in the "plugged" cell is connected to the emitter electrode. This connection provides additional drain to source capacitance that helps to stabilize the drain potential under short-circuit conditions. The result is stable oscillation free short-circuit operation even under high speed switching conditions. The waveform in Fig. 7 shows the typical low impedance short-circuit behavior of the PCM CSTBT chip. An added advantage of the PCM structure is its reduced input capacitance compared to conventional high cell density trench gate devices. Table 1 compares the key characteristics of the new PCM CSTBT chip to previous generation devices.

III. MEGA POWER DUAL™ PACKAGE

Most high power industrial inverters are based on conventional bridge configurations in which pairs of IGBTs (legs) are connected across a DC bus. In large inverters minimizing the inductance of this DC bus is critical for controlling transient voltages during switching. To simplify the design of this low inductance DC bus it is apparent that modules in a dual or half bridge configuration are advantageous. This is especially true if the modules internal inductance can be minimized to allow a simple two-layer laminated DC bus. Based on this concept a new high current dual package was developed. The new module called "MEGA POWER DUAL™" has an internal design and external configuration optimized for large industrial inverter applications.

Fig. 8 is a photograph of the new high current dual IGBT module. The package shown is designed to provide nominal collector current ratings of up to 1400A at 1200V and 1000A 1700V. The target applications include large industrial inverters for motor drive, UPS, and utility interface for alternate energy. Three of these dual modules can be used to provide about 0.5MW of output power. Multi-megawatt inverters can then be constructed by using either paralleled modules or inverter sub assemblies. The size and weight of system components in these large inverters is often a concern
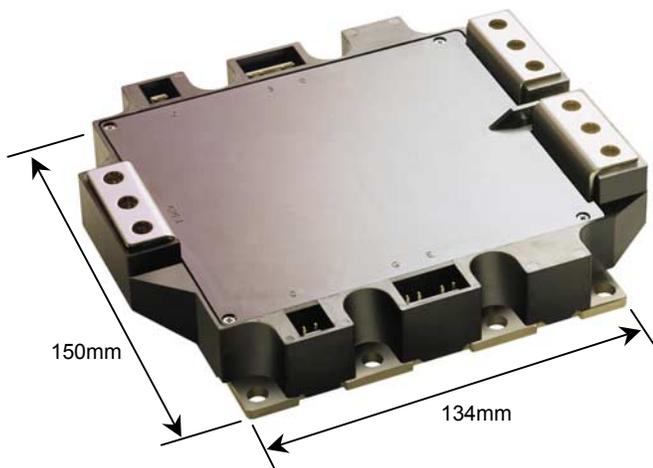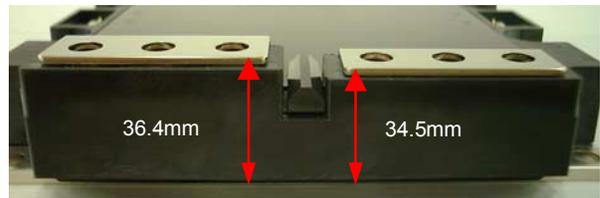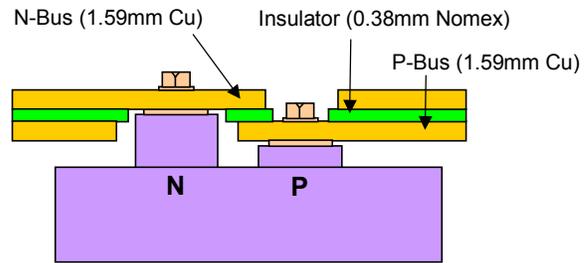

Figure 9 Offset step electrode structure

during assembly, shipping, and installation. The MEGA POWER DUAL™ module has been designed specifically to help reduce the size, weight, and cost of high power inverters. The superior performance of the new CSTBT chip enables a very compact package design with a footprint of only 150mm x 134mm. This is approximately half the size of an equivalent half bridge utilizing third generation IGBT modules. To help simplify laminated bus design the module's P and N terminals have a step offset of 1.9mm as shown in Fig. 9. The step allows simple planar buswork to be used. An example configuration for the bus plates and insulation material is also shown in Fig. 9. To minimize the weight and cost of the buswork it is desirable to utilize thinner copper sheet material. Wide, relatively thin, bus plates are usually more than capable of carrying the necessary current in high power inverters. However, thicker bus plates are often needed due to the local resistance at the bolted connections. To avoid this potential problem the new module utilizes large contact area three bolt power terminal
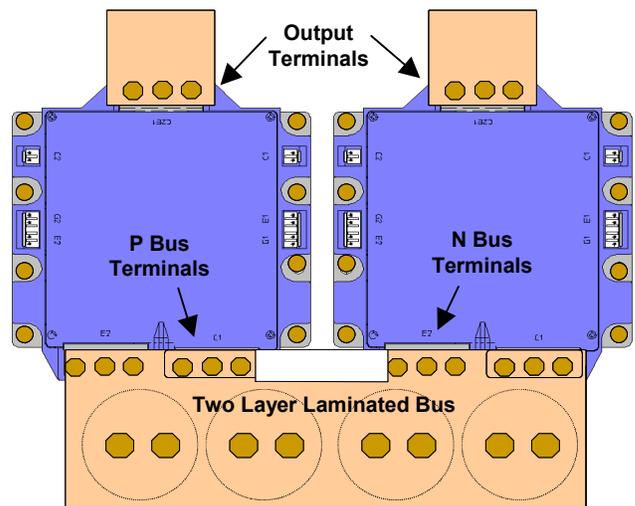

Figure 8 MEGA DUAL Package

Figure 10 Typical Power Bus Configuration
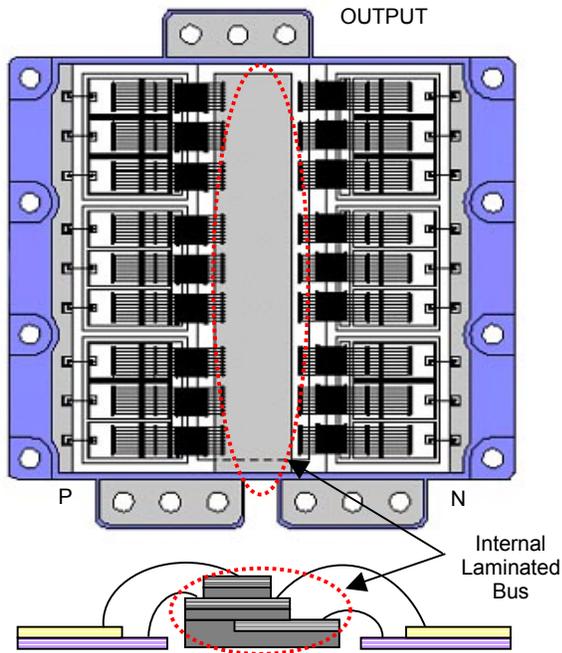
OUTPUT

P   N

Internal
Laminated
Bus

Figure 11 Internal Structure of New Module

connections. The module's power terminals have been located on the package in a "flow-through" pattern with the positive and negative bus connections on one end and the output connection on the opposite end. This configuration allows a simplified bus layout as shown in Fig. 10. In this structure a simple two layer laminated bus provides a low inductance connection from the main capacitor bank to the C1 and E2 terminals of the module. An important advantage of the "flow through" design is that it eliminates the need for the bus to extend over the module. This allows free access to
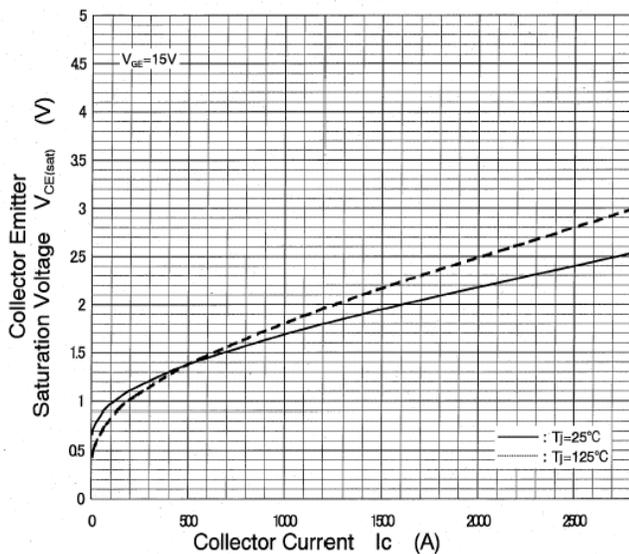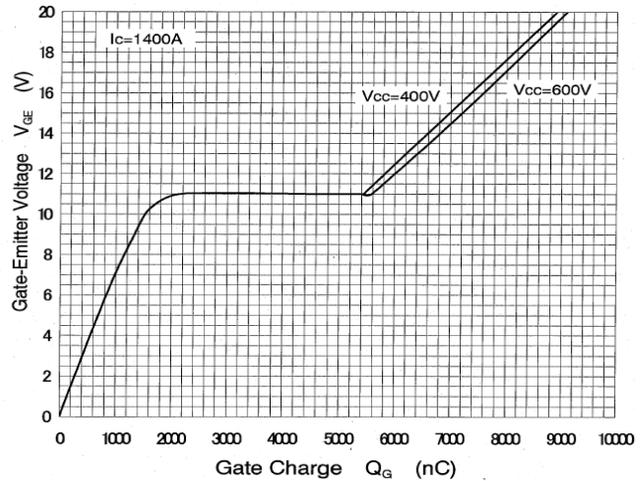

Figure 13 Gate Charge Characteristic

the gate connections and mounting bolts for simplified assembly and maintenance. It also helps to minimize the size and weight of the required buswork.

Another feature of the new package is recessed positive locking connectors for gate drive and collector potential sensing. These connectors allow the gate drive circuits to be easily installed after all heavy assembly is completed. This helps to reduce the risk of damage to the delicate gate drive components during assembly.

To help maintain low internal inductance the new module utilizes a unique three layer internal laminated bus structure as shown in Fig. 11. The laminated bus provides low impedance, simplified assembly and a symmetrical chip layout. An added advantage is that the chips are positioned in line with and close to the mounting bolts to provide superior heat transfer. Low thermal impedance is achieved through the use of AlN DBC ceramic isolation.
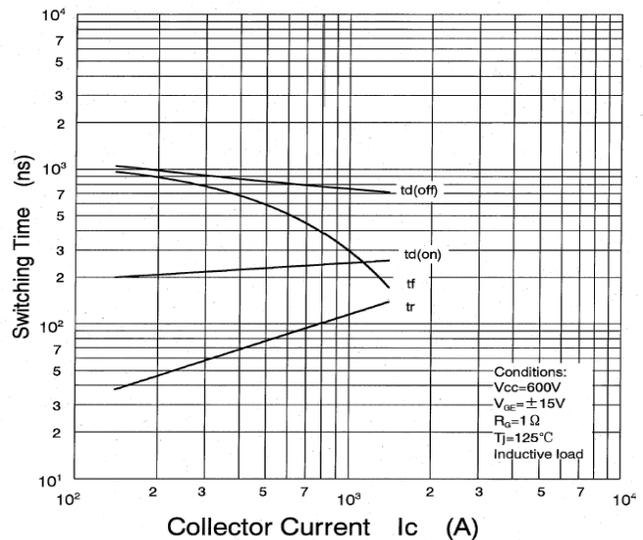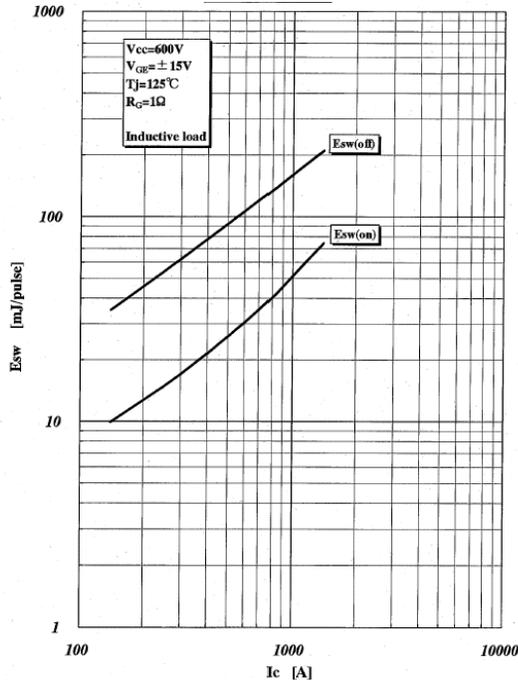

Figure 12 Saturation Voltage Characteristics

Figure 14 Half bridge Switching Characteristics

Figure 15 Switching Loss Characteristics

Figure 16 Transient Thermal Characteristic

IV. MEGA POWER DUAL^{TM} CHARACTERISTIC ANALYSIS

Fig. 12 shows the on-state voltage characteristic ($V_{CE(sat)}$) of the new 1400A, 1200V MEGA POWER DUAL^{TM} IGBT module. The low on-state voltage is the result of the CSTBT's stored carrier effect and its dramatic reduction of the PIN diode's resistance compared to a conventional IGBT structure. The on-state voltage of the PCM CSTBT chip is approximately the same as the narrow cell pitch trench gate IGBT (F-Series), demonstrating that the effect of the CSTBT structure overcomes the increase of the MOS channel resistance caused by the wider cell pitch. An advantage of the wide cell pitch CSTBT is its positive coefficient of saturation voltage. Fig. 12 shows that the $V_{CE(SAT)}$ will increase with increasing temperature at most normal operating currents. This characteristic allows simplified parallel operation and minimizes the risk of thermal run away conditions.

An added advantage of the wide cell pitch CSTBT is a large reduction in gate Miller capacitance. As shown in Table 1 the gate capacitance is about half of an equivalently rated forth generation trench gate device (F-Series). Fig. 13 shows the gate charge characteristic for the new 1400A, 1200V module. With +15V gate drive the total charge is about 7200nC which is only slightly more than a 600A, 1200V F-Series module.

Half bridge (inductive load) switching time characteristics are shown in Fig. 14. The fall and rise times at rated current are less than 200ns demonstrating that the CSTBT is suitable for operation frequencies in the 10kHz to 20kHz range. Fig.
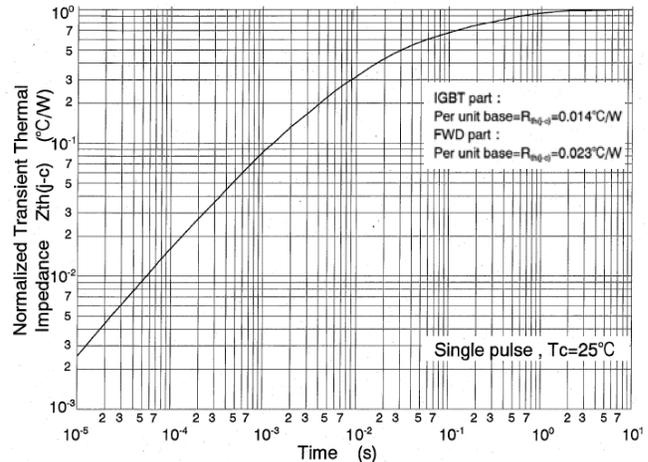
15 shows the switching energy characteristic. The low switching losses are the result of optimized n- and buffer layers in the CSTBT chip.

Fig. 16 shows the transient thermal impedance characteristic of the new module package. Low thermal impedance is achieved using 130W/mK aluminum nitride ceramic isolation material. This ceramic was selected because it offers more than five times better performance than the commonly used Alumina (Al_2O_3) ceramic. The module also employs a 4mm thick copper base for good transient thermal performance and lateral heat spreading.

V. CONCLUSION

A new high power dual IGBT module has been presented. The new module has a unique package optimized for high power industrial inverter applications. The module's mechanical configuration is optimized to allow simplified low cost assembly of high current power stages. The new module utilizes an advanced PCM CSTBT chip to provide low losses and rugged short-circuit performance.

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