USING F-SERIES IGBT MODULES

5.0 Introduction

Mitsubishi's new F-series IGBTs represent a significant advance over previous IGBT generations in terms of total power losses. The device remains fundamentally the same as a conventional IGBT, and the advice given in the application notes "General Considerations for IGBT and Intelligent Power Modules" and "Using IGBT Modules" should be observed. However the use of a trench-gate structure, and an integrated short circuit current control circuit, mean that there are sufficient differences in characteristics and behaviour to warrant further explanation.

5.1 Trench Gate IGBT Structure

Since the IGBT's introduction, successive generations of IGBT technology have featured steady improvements in on-state voltage and switching losses. However, improving the performance of existing IGBT technology has become increasingly difficult due to the constraints of the planar IGBT structure. The limitations of the planar IGBT arise partly from the resistance of the JFET region between adjacent cells in the MOSFET portion of the device, and partly from the forward voltage V_F of the diode structure in the bipolar portion of the device.

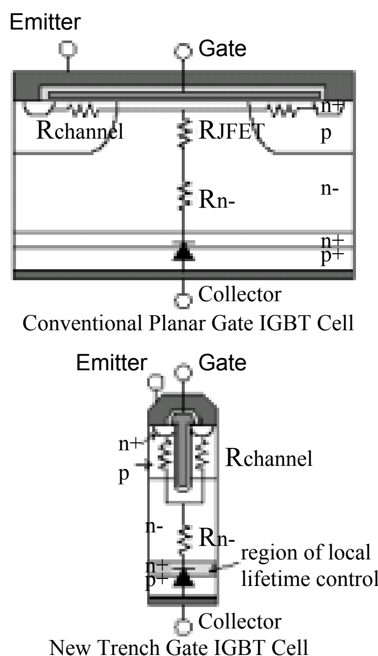
F-series IGBTs overcome the first constraint by utilising a trench gate structure, in which the gate oxide and conductive polysilicon gate electrode are formed in a deep narrow trench below the chip surface. The second limitation is addressed by using a new proton irradiation process.

Figure 5.1 shows a comparison of the structures of a conventional planar IGBT cell and a trench gate IGBT cell. This figure shows the components making up the on-state voltage drop, $V_{CE(sat)}$. Performance improvements realised in each of these compo-nents in the new structure are described below.

5.1.1 Reduction of Channel Resistance

When voltage is applied to the gate, the MOSFET channel forms along the vertical wall of the trench perpendicular to the surface of the chip. This is in contrast to the planar structure where the channel forms parallel to the chip surface. The vertical channel requires less chip area, permitting a substantial increase in cell density. The consequent increase in channel width per unit area results in a reduction in the $R_{channel}$ portion of the IGBT's on-state voltage drop.

Figure 5.1 Comparison of Trench and Planar IGBT Structures



Conventional Planar Gate IGBT Cell

New Trench Gate IGBT Cell

5.1.2 Elimination of JFET Region

The "JFET" resistance (R_{JFET}) in a planar IGBT exists due to the constriction of current flow in the region between adjacent cells. The trench gate structure effectively eliminates this region (Figure5.1). Furthermore, the non-uniform current density in the JFET region of planar IGBTs can lead to inconsistencies in the device SOA at high current densities. The trench structure achieves more uniform current flow which, combined with greater cell density, increases the rated current density compared with 1200V third generation planar.

5.1.3 V_F Reduction in Bipolar Region

The new IGBT is a punch through (PT) device, using a newly developed local lifetime control process. This proton irradiation technique allows carrier lifetime to be reduced in the n+ buffer layer only (Figure 5.1). Hence the turn-off losses can be reduced whilst maintaining a higher carrier lifetime in the n- drift region than was possible with the uniform lifetime control used in third generation planar IGBTs. This results in a greater carrier concentration in the drift region during conduction which reduces the R_{n-} component of $V_{CE(sat)}$.

5.2 Module Packaging

The F-series utilises Mitsubishi's innovative low inductance packaging technology, which

Figure 5.2 New package cross section

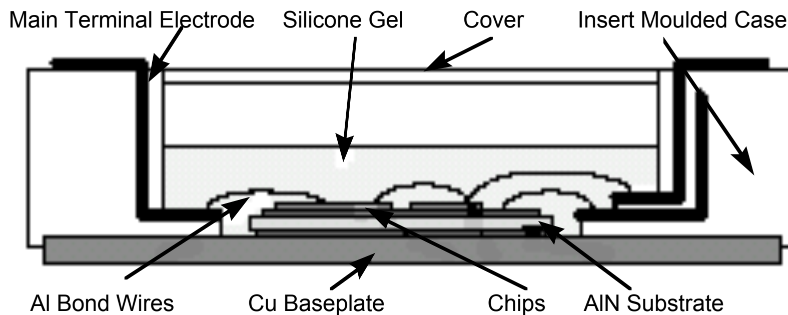
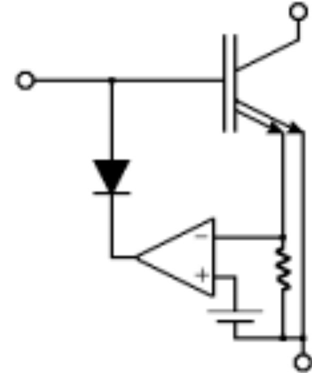


Figure 5.3 Simplified Diagram of RTC and IGBT Connection



was first introduced in the U-series range of planar IGBT modules. A cross-section of a typical module is shown in Figure 5.2.

The main power terminals are realised as a laminar busbar structure moulded into the side of the case. This gives much lower inductance than soldered electrodes, which are inserted into conventional modules after the case is moulded. In the new module, the terminals are wire bonded directly to the chips. The strain relieving S-bends needed in soldered electrodes are eliminated, further reducing the module inductance. This construction results in the module having about one-third the internal inductance of conventional modules.

Since no substrate area is required for soldering the electrodes, the total ceramic substrate area is reduced when compared with a conventional module. Thus aluminium nitride (AlN) ceramic, with lower thermal resistivity than aluminium oxide (Al_2O_3), can be economically used. Additionally, the parasitic capacitance of the module is reduced, increasing the impedance to high frequency noise between chip and heatsink.

In the manufacture of a conventional module a high temperature soldering process is used for chip to substrate and substrate to baseplate soldering. After case assembly, a second soldering process attaches the electrodes to the substrate. In the F-series module, this second step is not required. This in turn means that the first soldering step can be performed at lower temperature, reducing thermal stress during production.

5.3 RTC Description and Behaviour

F-series IGBTs include an integrated real-time current control (RTC) circuit for protection against short circuits, which was originally developed for intelligent power modules (IPMs). The RTC is a separate chip wire-bonded directly to the IGBT die and mounted adjacent to it. During normal operation of the device, the RTC is effectively “transparent” to the gate driver. It’s power supply is drawn from the main collector-emitter path of the IGBT, so it imposes no additional drain on the gate driver.

The RTC is connected to a current mirror emitter on the trench IGBT chip. A simplified diagram of this is shown in Figure 3. When the IGBT operates in a short circuit, the RTC detects the excessive current in the IGBT and reduces the gate-emitter voltage to limit the short-circuit current. The gate-emitter voltage is reduced to less than 12V, compared with the normal recommended value of 15V. The effect of gate-emitter voltage on short-circuit current is shown by Figure 5.4.

It is important to note that the RTC acts only to limit short-circuit current; it does not switch off the IGBT. Therefore the gate driver circuit should be designed to ensure that the IGBT is turned off within 10μs of a short circuit occuring.

The RTC limits the short circuit collector current to 2-4 times rated current, depending on the junction temperature of the IGBT and the short circuit di/dt. The minimum trip threshold for the RTC is 2 times the rated current of the device and occurs

Figure 5.4 Effect of Vge on Short Circuit Saturation Current of 150A, 1200V IGBT (without RTC)

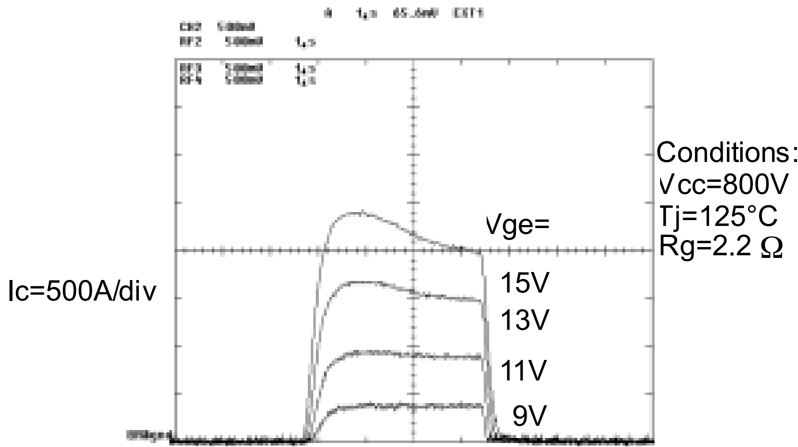
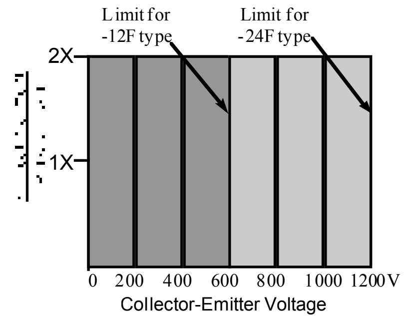


Figure 5.5 Switching SOA Diagram for F-series IGBT Modules



Conditions: Tj=25 - 125°C
Vge=+/-15V
Vcc=400V (-12F type)
800V (-24F type)

at high Tj and high di/dt. Therefore operation of the IGBT within its switching SOA is unaffected by the presence of the RTC.

5.4 Safe Operating Area

Safe operation of F-series IGBTs is governed by two safe operating areas (SOAs), defined at the main terminals of the device. These are the turn-off switching SOA governing repetitive switching operation, and the short circuit SOA governing non-repetitive operation.

5.4.1 Turn-off Switching SOA

The Switching SOA curve is the locus of points defining the maximum allowable simultaneous occurrence of collector current and collector to emitter voltage during turn-off. As seen in Figure 5.4, F-Series IGBTs offer square switching SOA up to 2x rated current for 600V and 1200V devices. This limit is defined by the designed current density of the chips and internal connections in the module.

Figure 5.6 Short Circuit SOA Diagram for 600V (-12F) F-series IGBT Modules

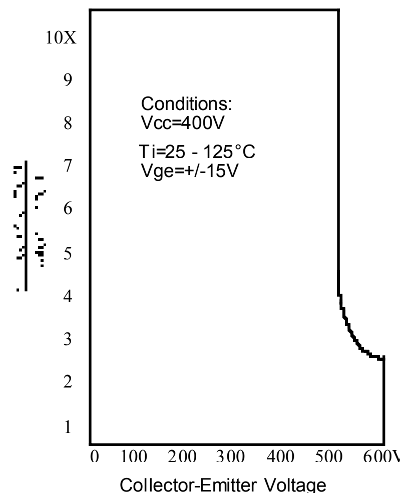
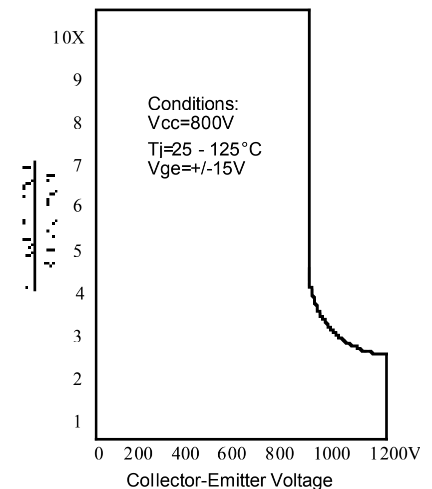


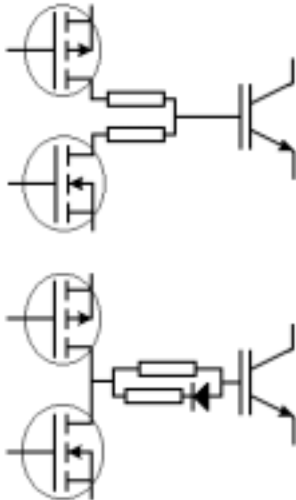
Figure 5.7 Short Circuit SOA Diagram for 1200V (-24F) F-series IGBT Modules



5.4.2 Short Circuit SOA

The short circuit SOA diagrams for F-series IGBTs are shown in Figures 5.6 and 5.7. These are identical to the equivalent diagrams for H- and U-series planar IGBT modules. In reality, however, the RTC limits current to less than the SOA limit of 10 times rated current, as described in section 5.3. Careful design of the power circuit and gate driver is necessary to ensure that the collector-emitter voltage limit is not exceeded. Note that the SCSOA of F-series IGBTs is applicable for pulse widths less than 10µs. The SCSOA is valid only for non-repetitive (“single shot”) operations.

Figure 5.8 Gate Drive Connections Giving Different Turn-on and Turn-off Gate Series Resistances



5.5 Gate Drive Requirements

F-series IGBTs are compatible with gate driver techniques and considering a specific gate driver circuits designed for planar IGBTs. When considering a specific gate driver circuit for application with an F-series module, the key parameters which will determine compatibility are the positive and negative bias voltages, the series gate resistance, the gate driver power source capability and the short circuit sensing method used.

5.5.1 Gate Drive Voltage

For turn-on a positive gate voltage of 15V ±10% is recommended. In no case should a gate drive outside of the range of 12 to 20V be used for turn-on.

In order to ensure that the IGBT stays in its off state when dv/dt noise is present in the collector-emitter voltage, an off bias must be used. Because the trench gate IGBT has a lower reverse transfer capacitance (C_{res}) than the planar type, a lower reverse bias voltage can be used. For F-series IGBTs a minimum reverse bias voltage of -2V is required to ensure immunity to dv/dt noise across the collector-emitter terminals.

Minimising the reverse bias voltage across the gate and emitter has the benefit of reducing the power which the gate driver must source to switch on the IGBT. However, using a larger reverse bias voltage decreases the turn-off delay time. This is particularly important in high frequency applications where a small deadtime is required. For the majority of low switching frequency (for example 5kHz or less) applications, -5V is a suitable value. In applications requiring a short deadtime -10V to -15V may be required, at the cost of an increase in gate driver power.

F-Series IGBT modules are not suitable for linear operation, due to the high gain of the device in the active region. Gate voltages in the 3 to 11V range should only appear on the IGBT's gate during rapid switching transitions.

5.5.2 Series Gate Resistance

Selection of the correct gate resistor values depends on a number of factors. The turn-on time and hence turn-on energy loss shows a strong dependence on the gate resistance. A smaller gate resistor results in faster switching and hence lower turn-off loss, but with the attendant disadvantage of higher di/dt and greater noise generation during reverse recovery of the freewheel diode. The turn-off time of the IGBT shows much less dependence on the gate resistance. However a smaller R_g results is a smaller turn-off delay time, and hence reduces the required deadtime. When considering the gate drive design, it is important to remember that a smaller R_g will mean that the gate driver must source a higher peak current during switching.

Some compromise between these requirements is inevitable when selecting the gate resistor. An increasingly common approach is to use different values for the turn-on and turn-off gate resistor values. Some examples of how to realise such a gate driver stage are shown in Figure 5.8. Such a circuit allows, for example, a relatively high R_g to be chosen for turn-on, in order to reduce the noise generated by the freewheel diode recovery, whilst a lower turn-off R_g reduces the turn-off delay and hence the necessary deadtime. Table 1 gives the recommended values of series gate resistance for F-series IGBT modules. All the switching data for the IGBT and freewheel diode given in the data sheet is specified using the minimum recommended gate resistor. The switching SOA and short circuit SOA for the device are valid for any gate resistance within the allowed range for a specific device.

5.5.3 Short Circuit Detection

It is possible to use the well known technique of $V_{ce(sat)}$ sensing for detecting a short

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Table 5.1 Series Gate Resistor Values for F-series IGBTs

Module type	Minimum gate resistor (Ω)	Maximum gate resistor (Ω)
600V		
CM75TU-12F	8.3	83
CM75DU-12F	8.3	83
CM100TU-12F	6.3	63
CM100DU-12F	6.3	63
CM150TU-12F	4.2	42
CM150DU-12F	4.2	42
CM200TU-12F	3.1	31
CM200DU-12F	3.1	31
CM300DU-12F	2.1	21
CM400DU-12F	3.1	31
CM600HU-12F	3.1	31
1200V		
CM50TU-24F	6.3	63
CM50DU-24F	6.3	63
CM75TU-24F	4.2	42
CM75DU-24F	4.2	42
CM100TU-24F	3.1	31
CM100DU-24F	3.1	31
CM150DU-24F	2.1	21
CM200DU-24F	1.6	16
CM300DU-24F	1.0	10
CM400DU-24F	0.78	7.8
CM400HU-24F	0.78	7.8
CM600HU-24F	1.0	10

Figure 5.9 Short Circuit Protection Using M57160L-01 Hybrid IC and V_{ge} sensing

Figure 5.10 IGBT Gate Charge Diagram

circuit of the IGBT. Another method of short circuit detection, made possible by the RTC, is used by the Mitsubishi M57160L-01 hybrid gate driver IC. This driver circuit senses a decrease in the gate-emitter voltage at the device terminals when the RTC becomes active. The short circuit protection is thus implemented without a connection to the collector of the IGBT using a fast-recovery diode. Figure 5.9 shows a gate driver circuit based on the M57160L-01 hybrid IC.

5.5.4 Gate Driver Power Requirements

The average power drawn from the gate driver power supply can be calculated using the gate charge characteristic (see Figure 5.10). The equation for calculating the gate power consumption, P_{AVG}, required of the supply is:

$$P_{AVG} = \Delta V_{GE} * Q_G * f$$

where

$\Delta V_{GE} = V_{GE(on)} + |V_{GE(off)}|$

Q_G = Total Gate Charge

f = Switching Frequency

Due to the higher gate-emitter capacitance of the trench gate IGBT structure, the power drain is much higher than for a planar device. For example, with a gate drive operating at +/-15V, the gate power requirement for 1200V F-series IGBTs is increased by a factor of 3 compared with their U-series equivalents.

5.6 Parallel Operation

To facilitate the matching of devices for parallel operation Mitsubishi provides IGBT modules marked with a saturation voltage rank letter. All devices to be operated in parallel should have the same saturation voltage rank. The saturation voltage rank will be either marked with white ink on the top of the module or indicated on the label. Saturation voltage ranking is normally available for modules rated 200A or higher. Modules of different saturation voltage ranks may be used in the same inverter provided that devices connected in parallel are of the same rank.

Table 5.2 shows the saturation voltage letter rankings for Mitsubishi F-series 600V and 1200V IGBT modules. Note that all ranks do not exist for a given voltage class. For example, 600V F-Series modules have a maximum data sheet saturation voltage of 2.2V and therefore rank P does not exist for these devices.

When modules of the same saturation voltage rank are paralleled the static current imbalance will be minimized so that the following recommended deratings can be applied:

600V F-Series derate Ic by 10%
1200V F-Series derate Ic by 15%

When more than two modules are paralleled the derating ratios in Table 5.3 should be applied.

Example:
In the case of four IGBT modules
of 600V class connected in parallel, the table gives a derating of 13.6%. So the derated current with 4 parallel 300A modules is:

300A(1 - 0.136) x 4 = 1037A

Table 5.2 $V_{ce(sat)}$ Rankings for Parallel Connection of F-series IGBTs

Vce(sat) at rated Ic, Tj=25°C, Vge=+15V	Parallel rank
1.50-1.60	E
1.55-1.65	F
1.60-1.70	G
1.65-1.75	H
1.70-1.80	J
1.75-1.85	K
1.80-1.95	L
1.90-2.05	M
2.00-2.20	N
2.15-2.40	P

Table 5.3 Derating ratios for Parallel Connection of F-series IGBTs

Number in parallel	Derating 600V	Derating 1200V
1	0	0
2	10%	15%
3	12.1%	17.4%
4	13.6%	19.6%
5	14.5%	20.9%
6	15.2%	21.7%

5.7 Switching Energy Characteristics

Switching energy curves are provided in order to simplify estimation of switching losses. Use of these curves is described in more detail in "USING IGBT MODULE".
Figure 5.11 and 5.13 shows turn-on and turn-off switching loss energy as a function of collector current.
Figure 5.12 and 5.14 show switching loss energy versus series gate resistance.
Figure 5.15 and 5.17 shows recovery switching loss energy of FWDi as a function of emitter current.
Figure 5.16 and 5.18 show recovery switching loss energy of FWDi versus series gate resistance.

Figure 5.11

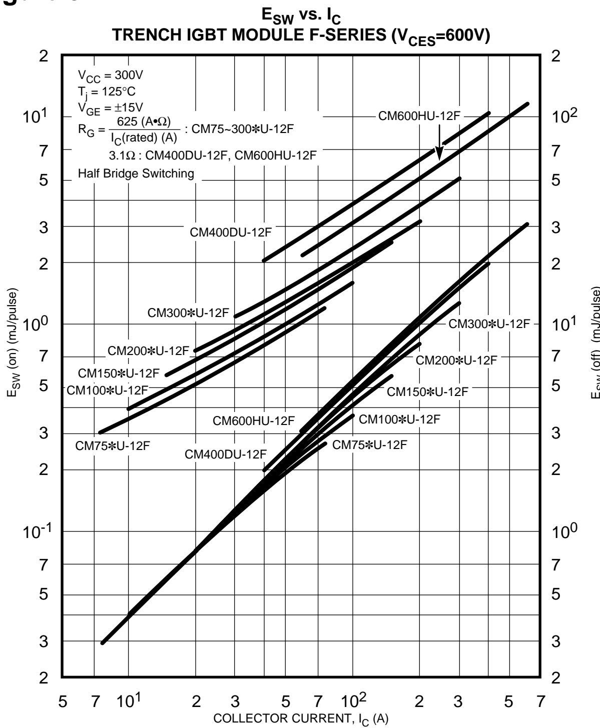

Figure 5.12

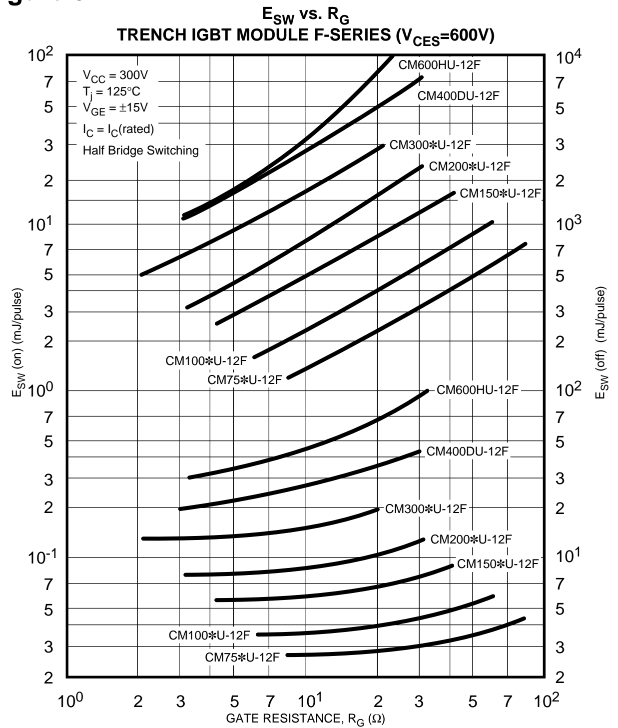

Figure 5.13

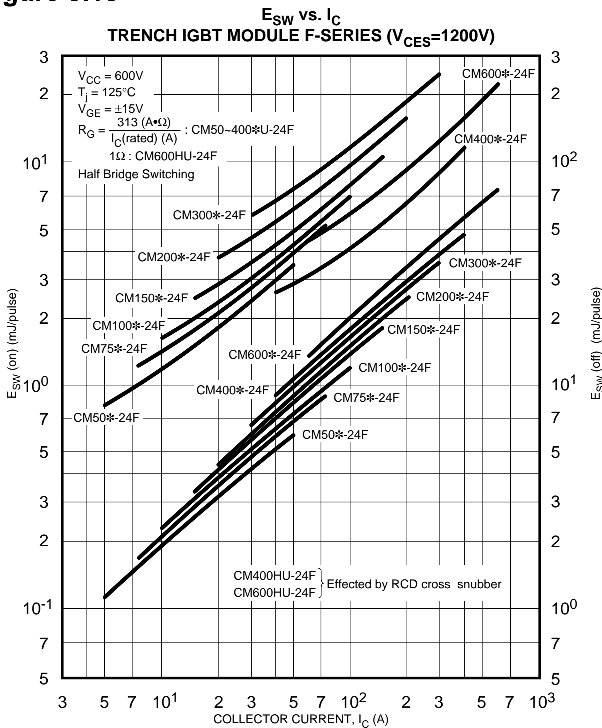

Figure 5.14

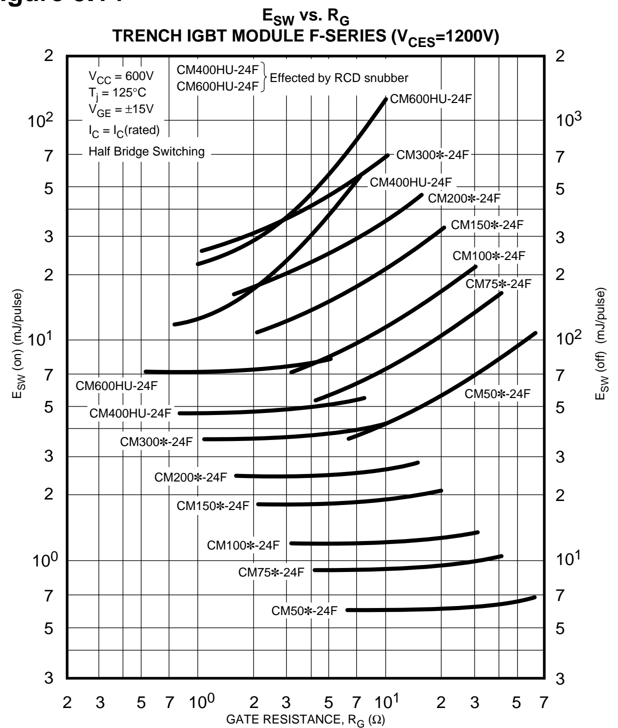

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Figure 5.15

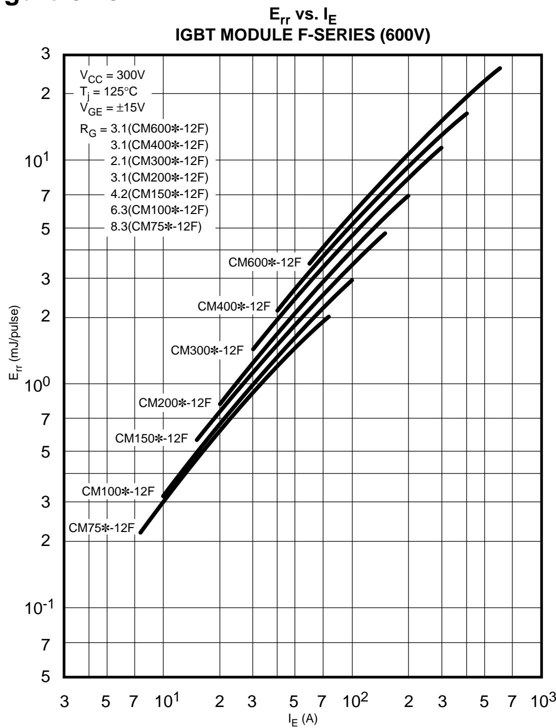

Figure 5.16

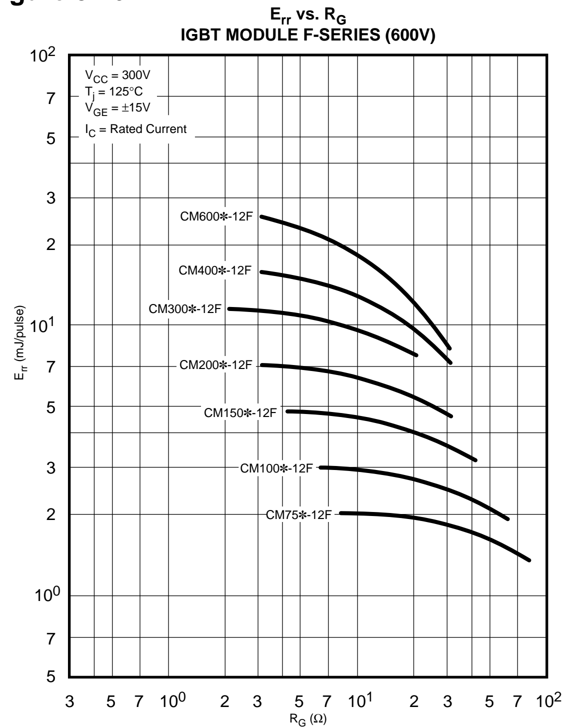

Figure 5.17

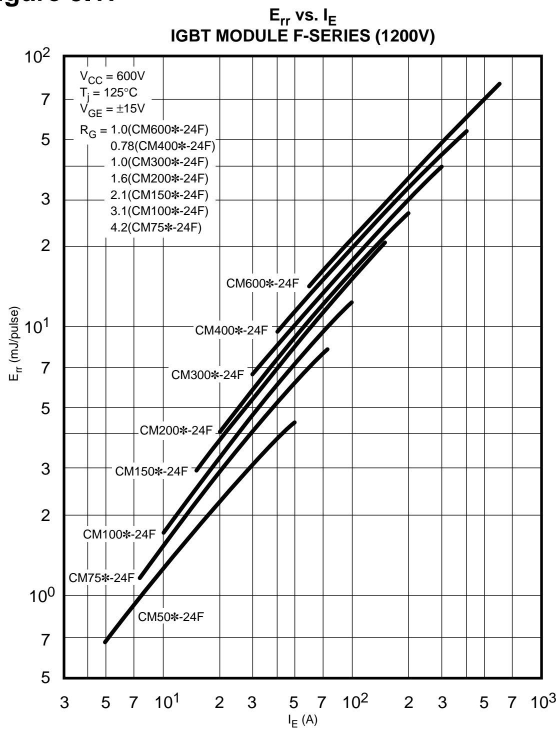

Figure 5.18