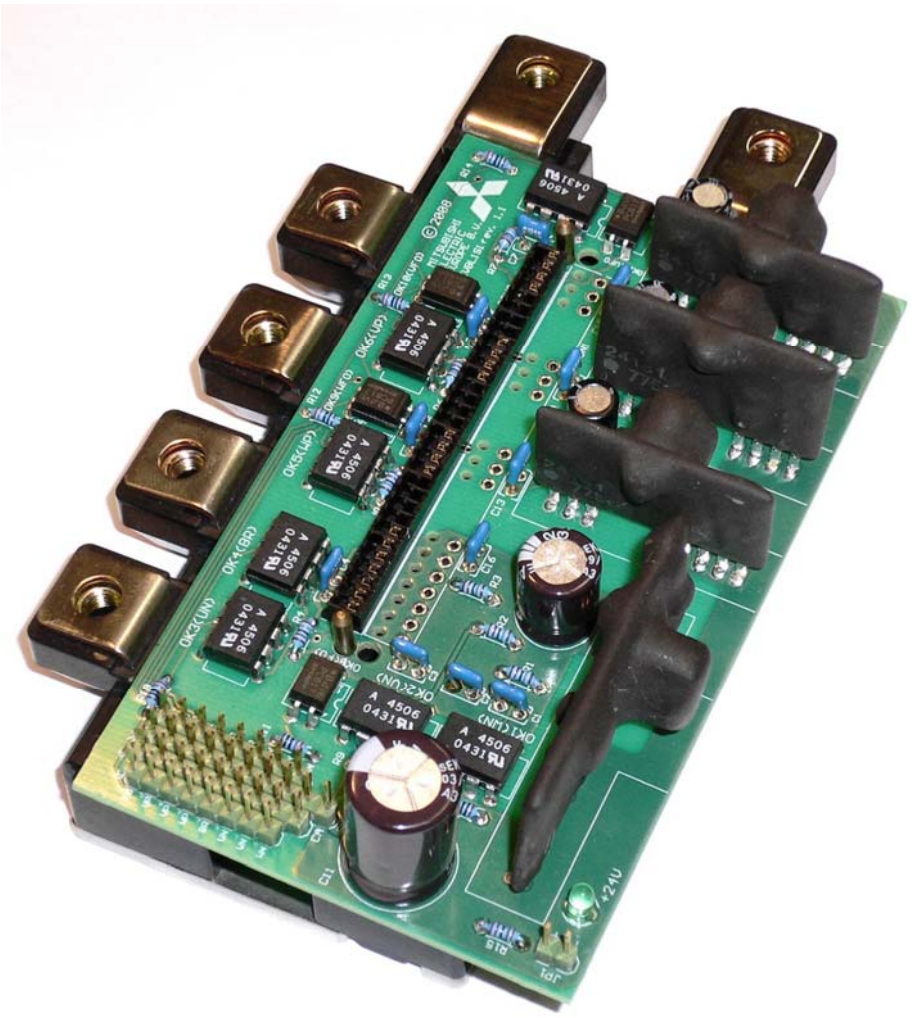
# L1S1-SERIES IPM
# EVALUATION BOARD
# (EVBL1S1XX)



EVBL1S1 mounted on an L1-series IPM
(2.54mm connector (S1) not placed in this prototype)

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***Caution: This evaluation board (EVB) is for testing purpose only. The evaluation board does not comply with any safety, isolation, environmental or EMI / EMC standard. Dangerous voltages can occur on the EVB and to equipment linked or connected to it. The operation should be carried out by qualified and authorized personnel only well respecting safety precautions.***

## 1. Introduction

The L1S1-series IPM evaluation board is intended to functionally test the features and the performance of the Mitsubishi L1S1-series Intelligent Power Modules. The L1 and S1 series is using FULL Gate CSTBT IGBT technology. The series contains 600V and 1200V device with a current range from 25A up to 300A. The EVBL1S1XX evaluation board can be used with all devices of the L1 and S1 series. Two different IPM connectors allow to use both the S1 and L1 devices. The control terminal pin assignment of the board is compatible with High-Active and Low-Active control signals and realized with a standard 2,54mm pin-header. Such 2,54mm pin-headers are available as a world wide standard. Only one power supply with 24V and recommended minimum of 300mA supply current capability is necessary to supply the Evaluation Board including the control and driver part of the IPM. The employed DC-DC converters ensure that the Evaluation Board power supply is completely isolated from IPM power supply. The DC-DC converter form in conjunction with the photocouplers a safety insulation barrier between control input of the evaluation board and the IPM's logic and supply.

The Evaluation Board's circuit is based on the interface and supply circuit which is recommended in the L1 and S1 IPM datasheets.

## 1.1 Application Example Circuit from the Datasheet:

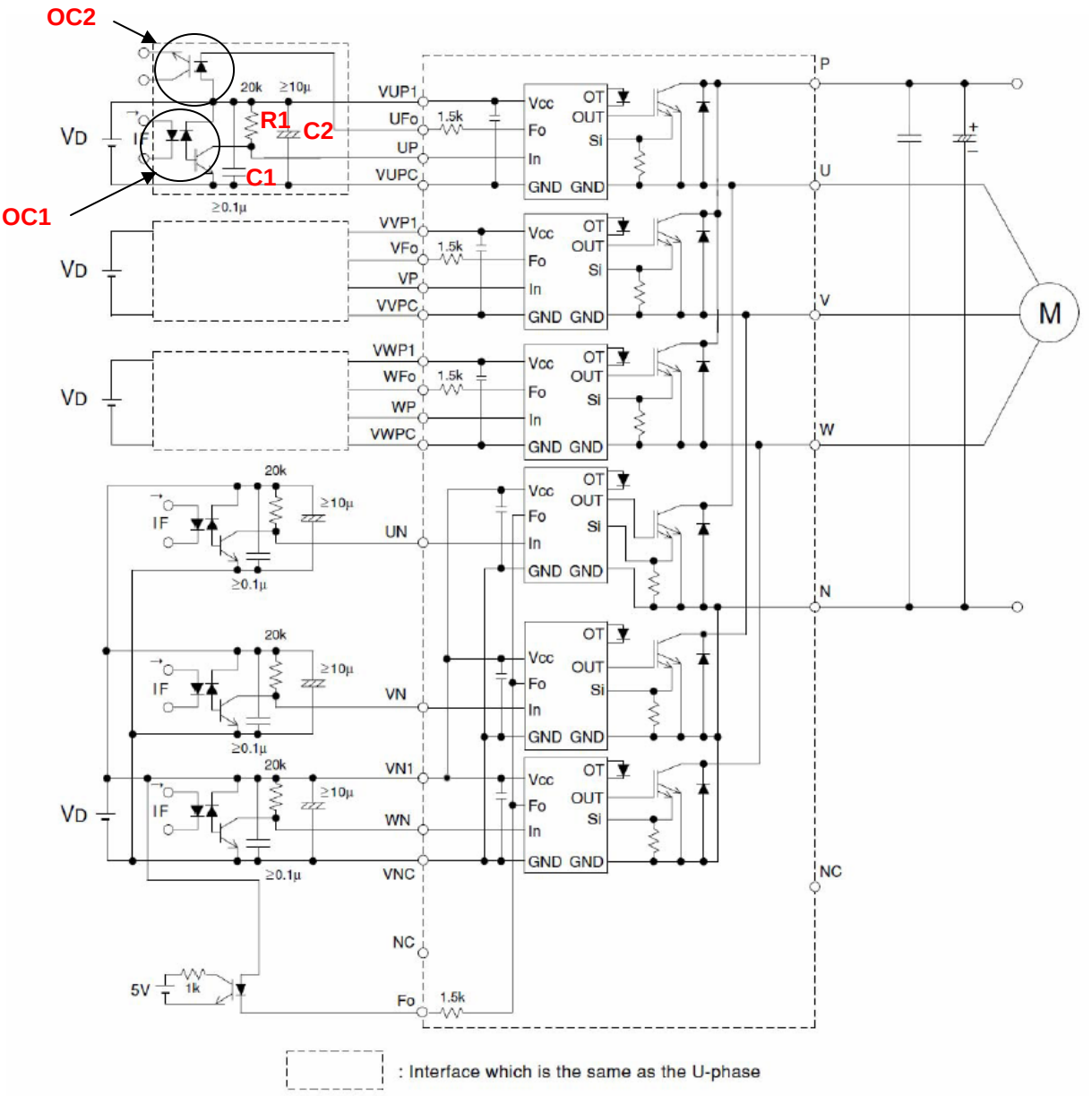



**figure 1: recommended interface circuit to L1/S1 IPM**

$V_D$ = isolated supply 15V
OC1 = fast safety photocoupler with high dv/dt CMR and isolation capability
OC2 = safety photocoupler for FO , high isolation and safety (VDE)
C1 = fast ceramic HF-benching capacitor ≥ 100nF/50V
C2 = enery storage longlife low ESR electrolytic capacitor ≥ 10µF/35V, $T_{max}$=105°C
R1 = 18kΩ…20kΩ pull up resistor

The Evaluation Board contains the isolated power supply and interface to control the IPM. The IPM itself is not part of the EVBL1S1 and must be ordered separately. To operate the IPM device in a basic application the following minimum additional hardware and the load itself is required.
Figure 2 shows the essential functional blocks to make the test setup operable:

## 1.2 Hardware requirements to use the IPM:

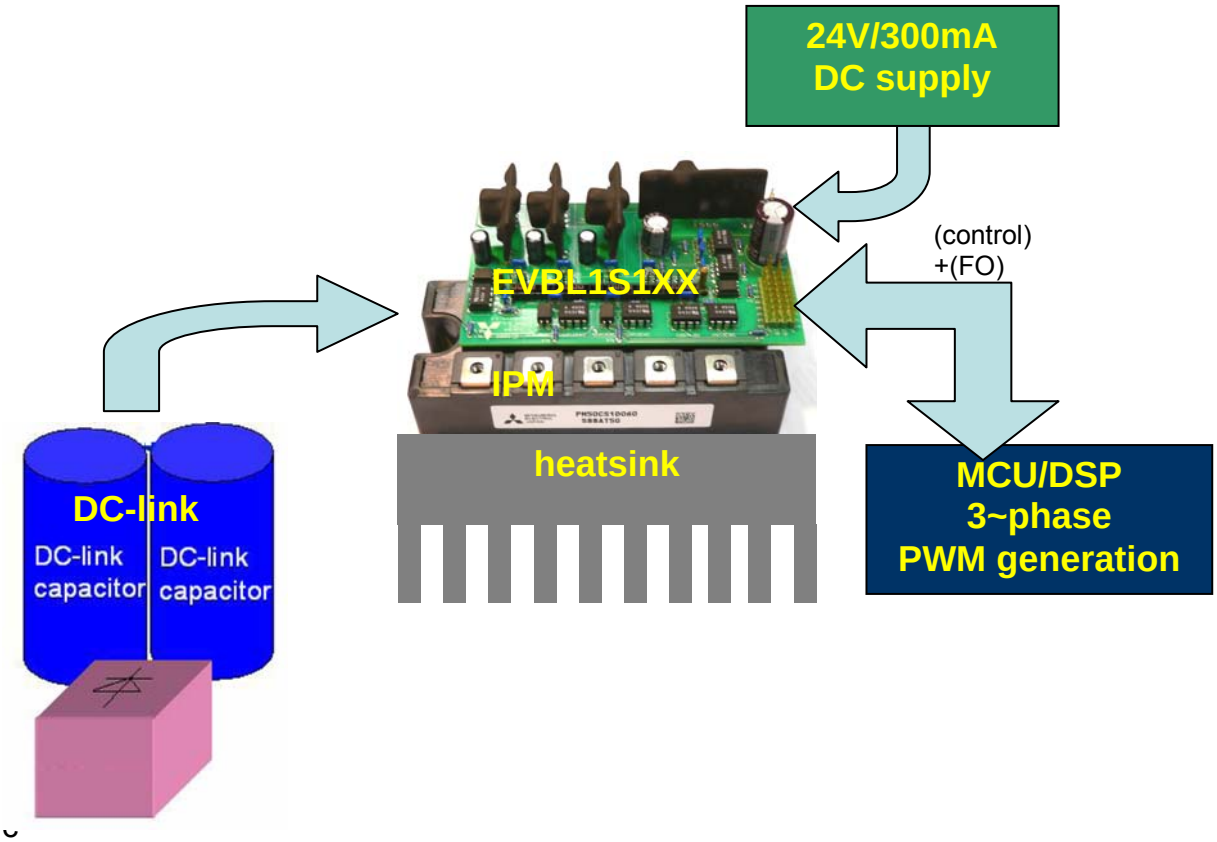



**figure 2: EVBL1S1XX and required application hardware for minimum operational test**

**Further information about the hardware requirements are given in the application note "USING INTELLIGENT POWER MODULES.**

(http://mitsubishichips.com/Global/files/manuals/powermos6_0.pdf)

## 2. Schematic of the Evaluation Board

Figure 3 is extracting the interface and supply circuit of the P-Side IGBT of leg U as an example of the structure of the entire board.

**Schematic UP Interface:**

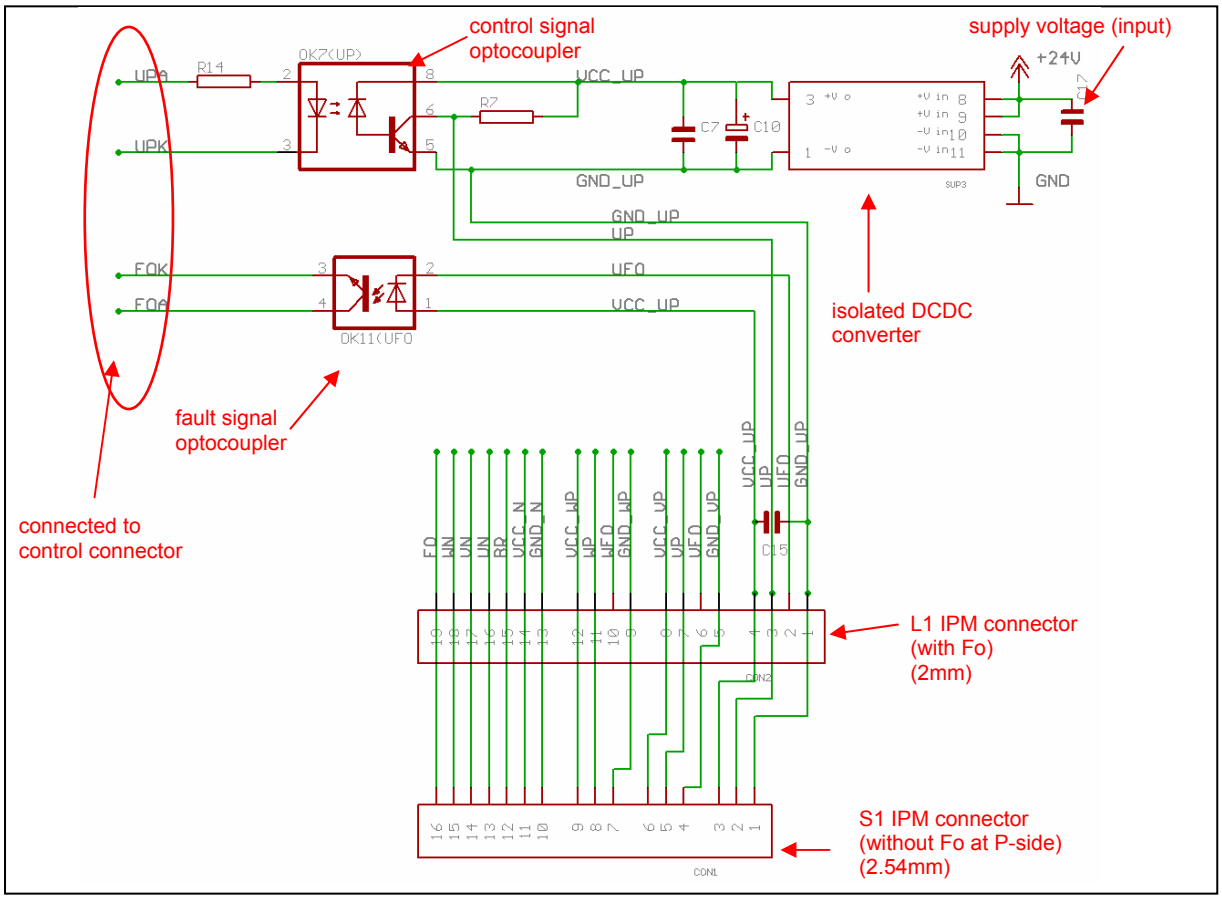



**figure 3: P-side phase"U"**

A high speed optocoupler (OK7) with high common mode rejection (CMR) is used for the signal input. The input pull-up resistor (R7=18k…20kΩ) has been selected to be low enough to avoid noise pick-up and to be high enough in resistance to allow the high speed phototransistor with a CTR of ~ 35% to pull the IPM input below the recommended maximum $V_{CIN(on)}$ threshold voltage, e.g. to turn on the IPM safely.
A low speed optocoupler with safety approval is used to transfer the fault outputs (Fo) of the IPM to the insulated side. Decoupling capacitors C7,C17 and C15 are used to avoid malfunctions caused by noise and C10, the electrolytic capacitor, provides the energy reservoir for the floating side. Such kind of noise is mainly created by the fast switching IGBTs and the resulting high dv/dt and di/dt.

The L1 and S1 connectors allow to use both IPM series and provide an easy installation of the evaluation board.

In figure 4 the complete evaluation board schematic is shown.

## 2.1 Schematic of the whole evaluation board:

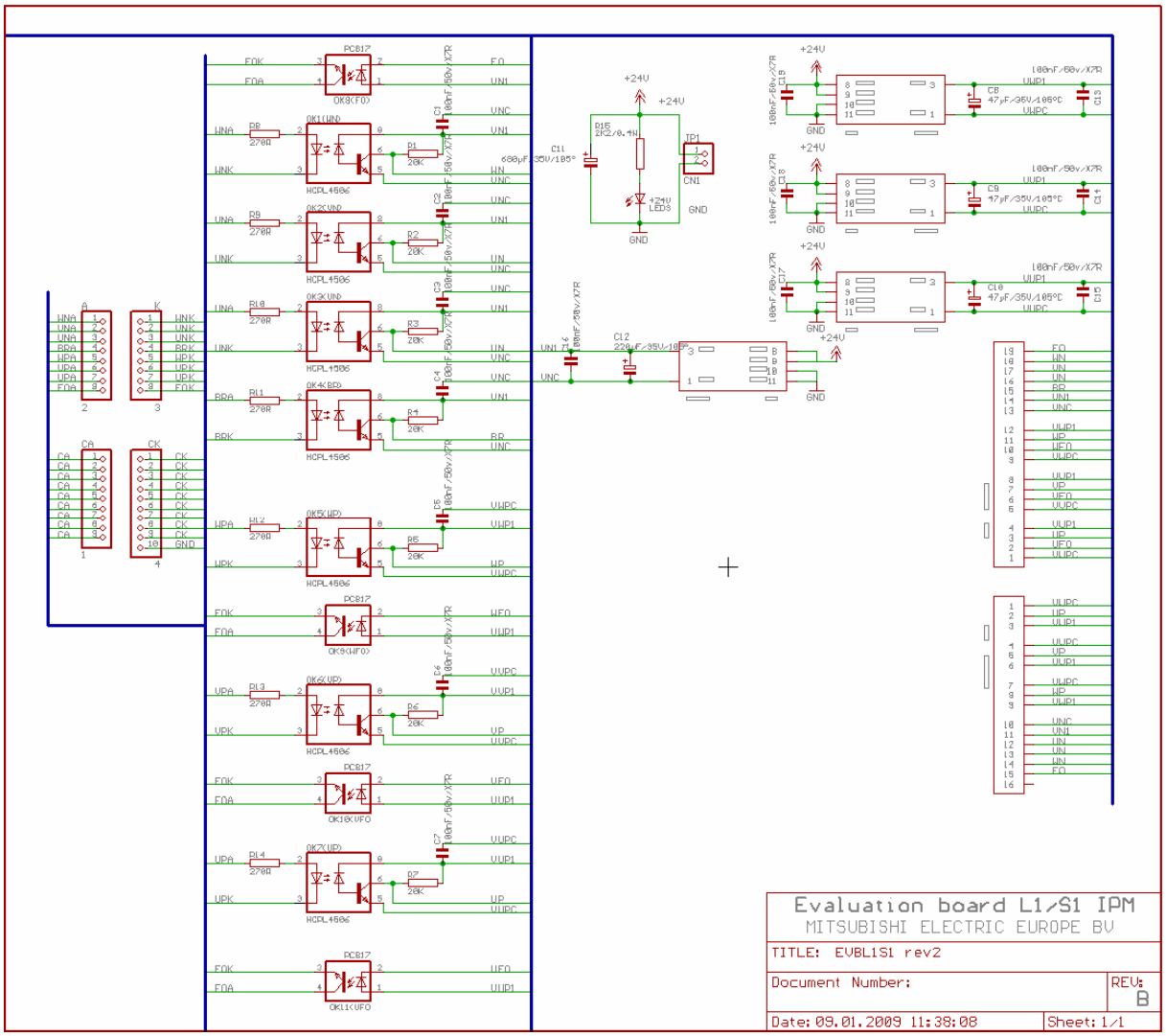


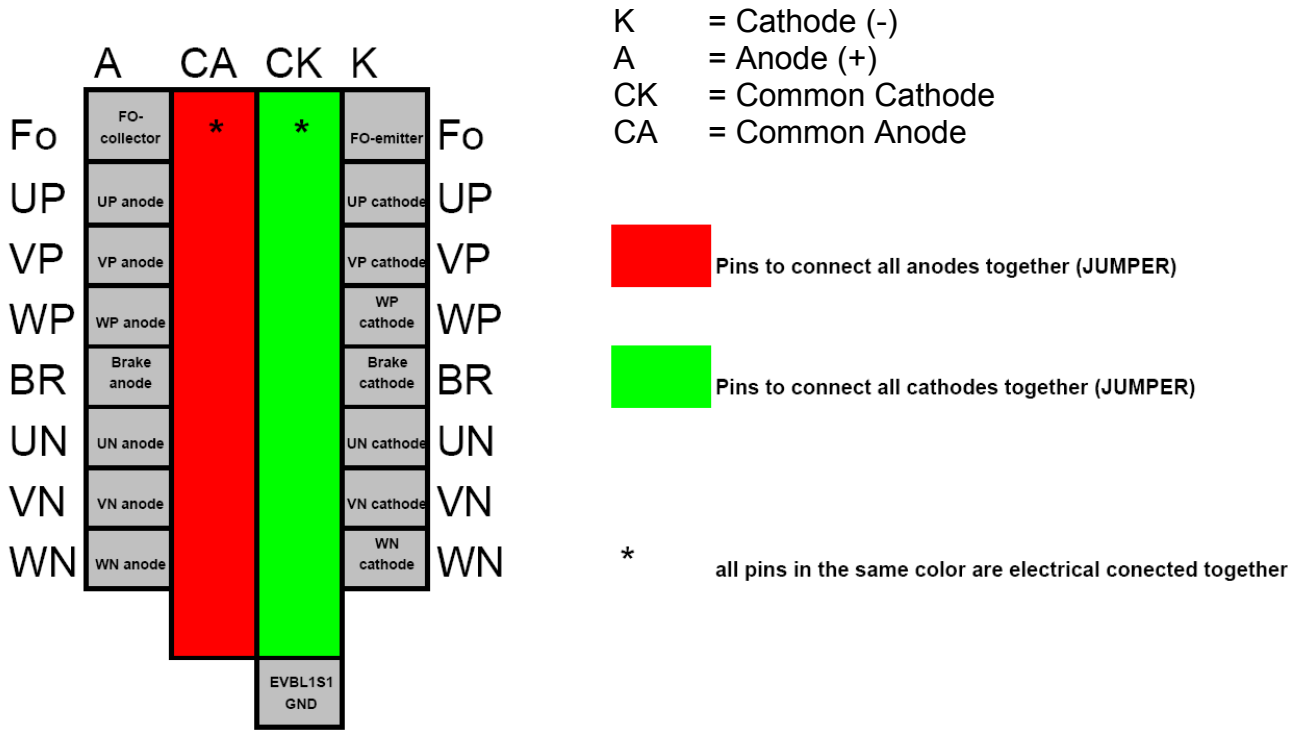

**figure 4: complete schematic of the evaluation board**

The schematic according to figure 4 reveals the simplicity of the interface circuit to drive the IPM. Indeed by the high degree of integration in the IPM itself which provides the driver and complete protection functions like under voltage, over temperature sensor on each IGBT chip, the total external circuitry becomes simple.

## 3. Control interface connector

The control terminal pin assignment of the board is compatible with High-Active and Low-Active control signals and realized with a standard 2,54mm pin-header array. The series resistor of the input high speed optocoupler diode is dimensioned as 270Ω for a recommended control input voltage of 5V.
All cathodes and anodes of the input high speed optocoupler are connected through these 270R resistances to the pin-header. The pin-header contains only one Emitter and Collector pin as a sum signal of all fault output phototransistors. The following examples describe how to connect the evaluation board for high active and low active PWM signals.

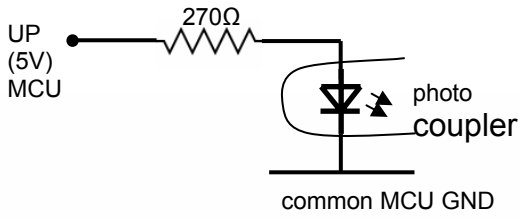
### 3.1 General connector description:



### 3.2 configuration for high active PWM:

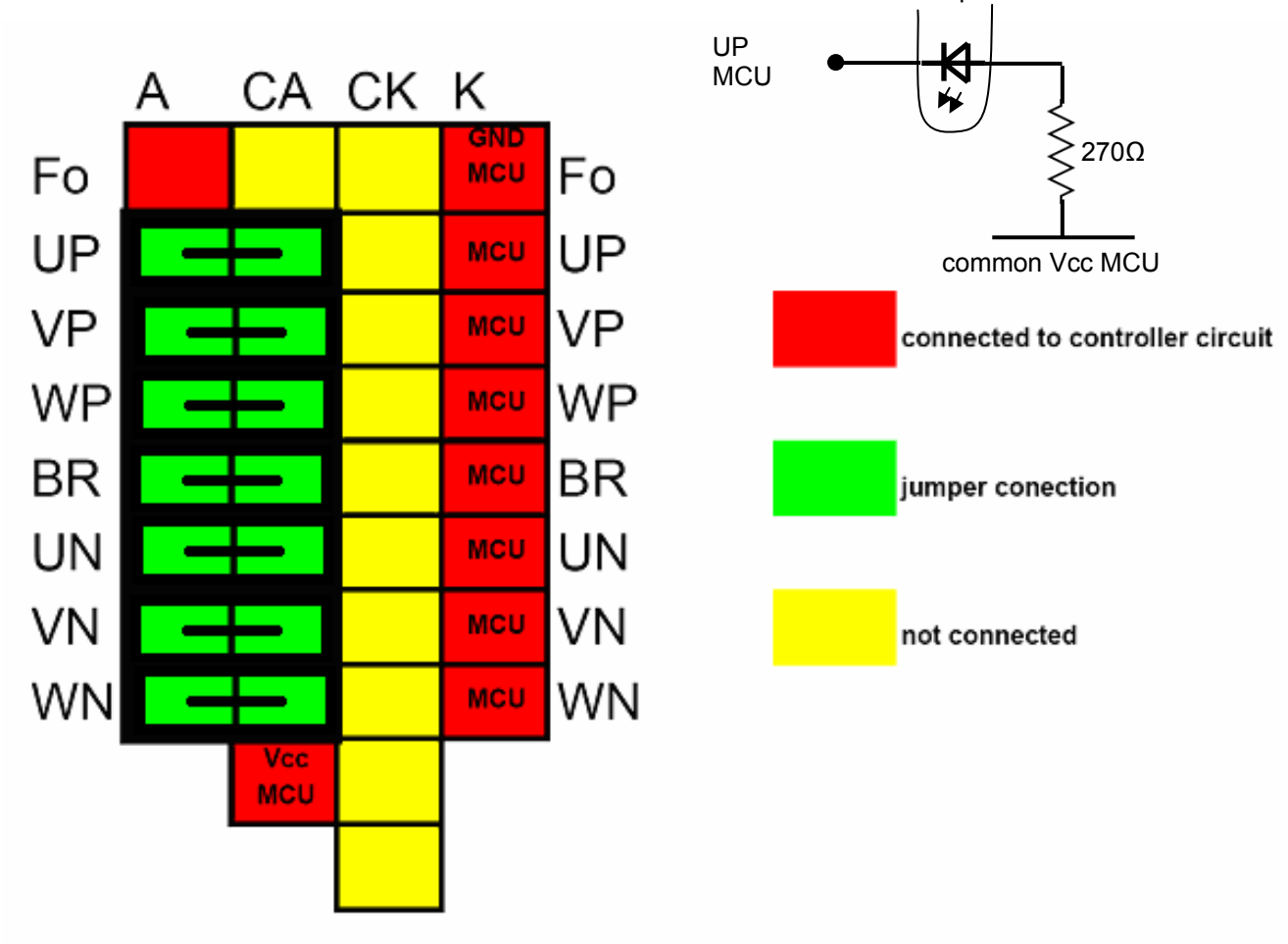
“CK” is connected to “K” by jumpers.

**example channel (UP):**

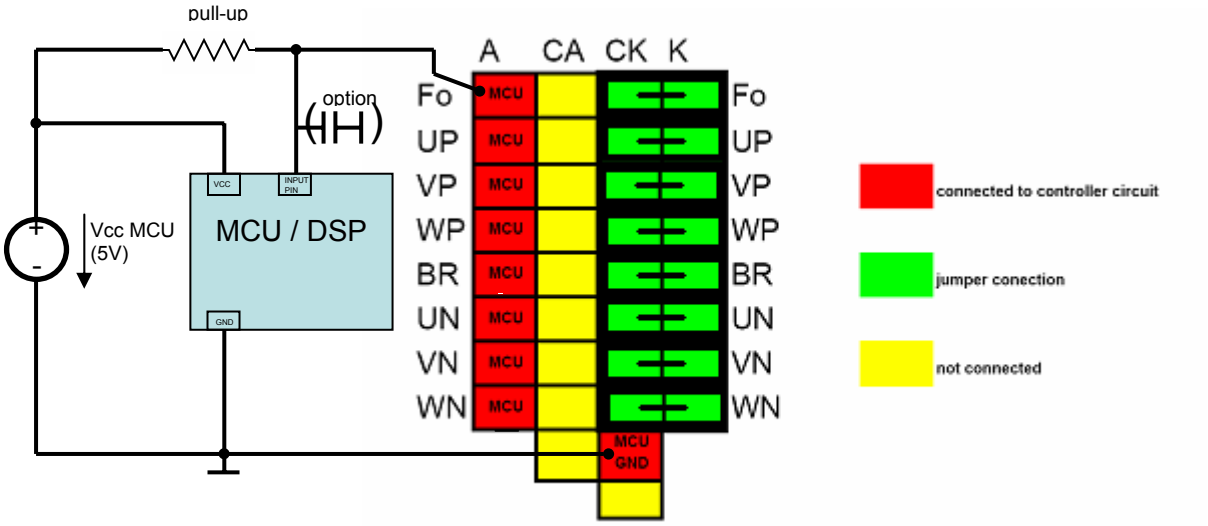


### 3.3. Configuration for low active PWM example:

“CA” is connected to “A” by jumpers.



### 3.4 Fault output (Fo) example:

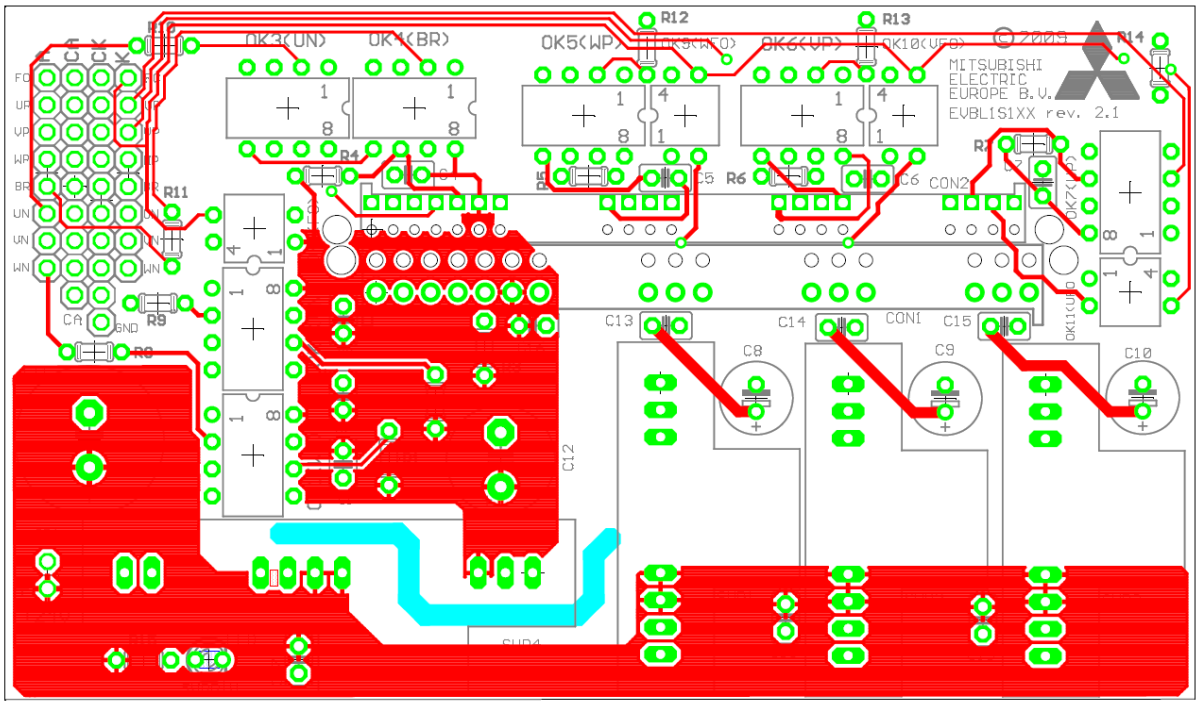



In this example the fault output signal at the input of the MCU/DSP is low active. Referring to the example 3.2 a high active Fo can be generated, too.

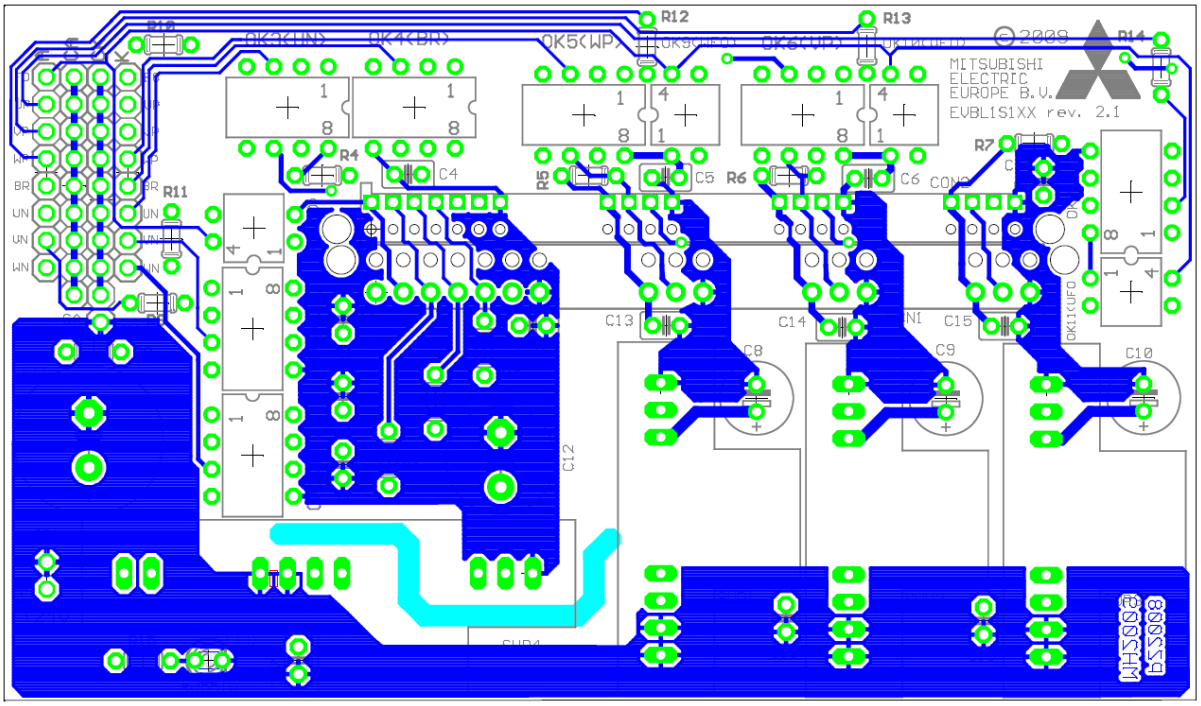
Removing the jumper from “CK” to “K” and connecting instead “K” of “Fo” to the reference point on the µC’s PCB would allow to provide a potential free Fo detection. This 2-wire potential free connection to the µC board can have substantial advantages regarding EMI sensitivity of the fault detection logic on the µC board by avoiding GND- loops.

## 4. PCB

**Toplayer:**




**Bottomlayer:**




Both layers show a clear separation of traces having different potentials. The layout tries to realize shortest traces between electrical connections and provide a maximum of clearance and creepage distances considering the given space of the PCB fitting on op of the IPM.

## 5. Bill of material (BOM)

| Name | Value | Package | Supplier |
|---|---|---|---|
| C1 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C2 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C3 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C4 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C5 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C6 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C7 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C8 | 47µF/35V/105°C | E2,5-7 | |
| C9 | 47µF/35V/105°C | E2,5-7 | |
| C10 | 47µF/35V/105°C | E2,5-7 | |
| C11 | 680µF/35V/105°C | E5-13 | |
| C12 | 220µF/35V/105°C | E5-10,5 | |
| C13 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C14 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C15 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C16 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C17 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C18 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| C19 | 100nF/50v/X7R | C2,5-2 | EPCOS B37987M5104k54 |
| CON1 | HRS R 254 | 2,54mm pitch | Hirose |
| CON2 | HRS L 2 | 2,00mm pitch | Hirose |
| OK1(WN) | HCPL4506 | DIL08 | Avago |
| OK2(VN) | HCPL4506 | DIL08 | Avago |
| OK3(UN) | HCPL4506 | DIL08 | Avago |
| OK4(BR) | HCPL4506 | DIL08 | Avago |
| OK5(WP) | HCPL4506 | DIL08 | Avago |
| OK6(VP) | HCPL4506 | DIL08 | Avago |
| OK7(UP) | HCPL4506 | DIL08 | Avago |
| OK8(FO) | PC817 | DIL04 | SHARP |
| OK9(WFO) | PC817 | DIL04 | SHARP |
| OK10(VFO | PC817 | DIL04 | SHARP |
| OK11(UFO | PC817 | DIL04 | SHARP |
| R1 | 18k…20k | 0204/5 | |
| R2 | 18k…20k | 0204/5 | |
| R3 | 18k…20k | 0204/5 | |
| R4 | 18k…20k | 0204/5 | |
| R5 | 18k…20k | 0204/5 | |
| R6 | 18k…20k | 0204/5 | |
| R7 | 18k…20k | 0204/5 | |
| R8 | 270R | 0204/5 | |
| R9 | 270R | 0204/5 | |
| R10 | 270R | 0204/5 | |
| R11 | 270R | 0204/5 | |
| R12 | 270R | 0204/5 | |
| R13 | 270R | 0204/5 | |
| R14 | 270R | 0204/5 | |
| R15 | 2K2/0.4W | 0204/5 | |
| SUP1 | VLA24151 | VLA15151 | Isahaya |
| SUP2 | VLA24151 | VLA15151 | Isahaya |
| SUP3 | VLA24151 | VLA15151 | Isahaya |
| SUP4 | VLA24154 | VLA24154 | Isahaya |

## 6. Disclaimer

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4. We do not warrant uninterrupted or error free operation of the evaluation board and all related hardware.
5. We have no obligation to provide service, defect correction, or any maintenance for the L1S1-series IPM evaluation board.
6. We have no obligation to supply any updates or enhancements to you even if such are or later become available.

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