MITSUBISHI <INTELLIGENT POWER MODULES>
PM100CLA120
FLAT-BASE TYPE
INSULATED PACKAGE

PM100CLA120

FEATURE
a) Adopting new 5th generation IGBT (CSTBT) chip, which performance is improved by 1µm fine rule process.
For example, typical Vce(sat)=1.9V @Tj=125°C
b) I adopt the over-temperature conservation by Tj detection of CSTBT chip, and error output is possible from all each conservation upper and lower arm of IPM.
- 3φ100A, 1200V Current-sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
- Acoustic noise-less 18.5kW/22kW class inverter application
- UL Recognized Yellow Card No.E80276(N)
  File No.E80271

APPLICATION
General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES Dimensions in mm

Terminal code
1. VUPC  6. VFO 11. WP 16. UN
2. UFO  7. VP 12. VWP1 17. VN
3. UP  8. VVP1 13. VNC 18. WN
4. VUP1  9. VWPC 14. VN1 19. Fo
5. VVPC 10. WFO 15. NC

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MAXIMUM RATINGS \( (T_{j} = 25^\circ \text{C}, \text{unless otherwise noted}) \)

### INVERTER PART

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCES</td>
<td>Collector-Emitter Voltage</td>
<td>( V_d = 15 \text{V}, V_{\text{CIN}} = 15 \text{V} )</td>
<td>1200</td>
<td>V</td>
</tr>
<tr>
<td>hC</td>
<td>Collector Current</td>
<td>( T_c = 25^\circ \text{C} )</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td>hCP</td>
<td>Collector Current (Peak)</td>
<td>( T_c = 25^\circ \text{C} )</td>
<td>200</td>
<td>A</td>
</tr>
<tr>
<td>Pc</td>
<td>Collector Dissipation</td>
<td>( T_c = 25^\circ \text{C} ) (Note-1)</td>
<td>781</td>
<td>W</td>
</tr>
<tr>
<td>( T_j )</td>
<td>Junction Temperature</td>
<td></td>
<td>(-20 \sim +150 )</td>
<td>({}^\circ \text{C})</td>
</tr>
</tbody>
</table>

### CONTROL PART

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vd</td>
<td>Supply Voltage</td>
<td>Applied between : ( V_{\text{UP1}}-V_{\text{UPC}} ) ( V_{\text{VP1}}-V_{\text{VPC}} ) ( V_{\text{WP1}}-V_{\text{WPC}} ), ( V_{\text{VN1}}-V_{\text{VNC}} )</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>V_{\text{CIN}}</td>
<td>Input Voltage</td>
<td>Applied between : ( V_{\text{UP1}}-V_{\text{UPC}} ) ( V_{\text{VP1}}-V_{\text{VPC}} ) ( V_{\text{WP1}}-V_{\text{WPC}} ), ( V_{\text{VN1}}-V_{\text{VNC}} )</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>VFO</td>
<td>Fault Output Supply Voltage</td>
<td>Applied between : ( V_{\text{FO}}-V_{\text{UPC}} ), ( V_{\text{FO}}-V_{\text{VPC}} ), ( V_{\text{FO}}-V_{\text{WPC}} ), ( V_{\text{FO}}-V_{\text{VNC}} )</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>IFO</td>
<td>Fault Output Current</td>
<td>Sink current at ( V_{\text{FO}}, V_{\text{FO}}, W_{\text{FO}}, F_{\text{O}} ) terminals</td>
<td>20</td>
<td>mA</td>
</tr>
</tbody>
</table>
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INSULATED PACKAGE

TOTAL SYSTEM

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC(PROT)</td>
<td>Supply Voltage Protected by SC</td>
<td>V_D = 13.5 ~ 16.5V, Inverter Part, T_j = +125°C Start</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>VCC(surge)</td>
<td>Supply Voltage (Surge)</td>
<td>Applied between P-N, Surge value</td>
<td>1000</td>
<td>V</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature</td>
<td>–40 ~ +125°C</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Viso</td>
<td>Isolation Voltage</td>
<td>60Hz, Sinusoidal, Charged part to Base, AC 1 min.</td>
<td>2500</td>
<td>Vrms</td>
</tr>
</tbody>
</table>

THERMAL RESISTANCES

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rth(j-c)</td>
<td>Junction to case Thermal Resistances</td>
<td>Inverter IGBT (per 1 element) (Note-1)</td>
<td>— — 0.16*</td>
<td>°C/W</td>
</tr>
<tr>
<td>Rth(c-f)</td>
<td>Contact Thermal Resistance</td>
<td>Case to fin, (per 1 module) Thermal grease applied (Note-1)</td>
<td>— — 0.023</td>
<td></td>
</tr>
</tbody>
</table>

* If you use this value, Rth(j-a) should be measured just under the chips.

(Note-1) Tc (under the chip) measurement point is below.

(Unit : mm)

<table>
<thead>
<tr>
<th>arm</th>
<th>axis</th>
<th>IGBT</th>
<th>FWDi</th>
<th>IGBT</th>
<th>FWDi</th>
<th>IGBT</th>
<th>FWDi</th>
<th>IGBT</th>
<th>FWDi</th>
<th>IGBT</th>
<th>FWDi</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>23.7</td>
<td>23.0</td>
<td>57.2</td>
<td>56.5</td>
<td>87.7</td>
<td>86.5</td>
<td>37.7</td>
<td>38.0</td>
<td>70.2</td>
<td>71.5</td>
<td>100.7</td>
</tr>
<tr>
<td>Y</td>
<td>56.7</td>
<td>43.4</td>
<td>56.7</td>
<td>43.4</td>
<td>56.7</td>
<td>43.4</td>
<td>28.7</td>
<td>42.0</td>
<td>28.7</td>
<td>42.0</td>
<td>28.7</td>
</tr>
</tbody>
</table>

Bottom view

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCE(sat)</td>
<td>Collector-Emitter Saturation Voltage</td>
<td>V_D = 15V, I_C = 100A</td>
<td>— 1.6 2.3</td>
<td>V</td>
</tr>
<tr>
<td>VCE</td>
<td>FWDi Forward Voltage</td>
<td>–I_C = 100A, V_D = 15V, V_CEIN = 15V (Fig. 1)</td>
<td>— 2.5 3.5</td>
<td>V</td>
</tr>
<tr>
<td>boF</td>
<td>Forward Voltage</td>
<td>V_D = 15V, V_CEIN = 0V→15V</td>
<td>0.5 1.0 2.5</td>
<td>µs</td>
</tr>
<tr>
<td>toF</td>
<td>Switching Time</td>
<td>V_D = 600V, I_C = 100A</td>
<td>— 0.4 1.0</td>
<td>µs</td>
</tr>
<tr>
<td>toe</td>
<td>Inductive Load</td>
<td>T_j = 125°C (Fig. 3, 4)</td>
<td>— 2.0 3.0</td>
<td></td>
</tr>
<tr>
<td>tcoF</td>
<td>Cutoff Current</td>
<td>V_CE = V_CEIN, V_CEIN = 15V (Fig. 5)</td>
<td>— 0.7 1.2</td>
<td>mA</td>
</tr>
</tbody>
</table>

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CONTROL PART

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Id</td>
<td>Circuit Current</td>
<td>$V_D = 15V, V_{CN} = 15V$</td>
<td>$V_{N1-NC}$</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{P1-P1}$</td>
<td>—</td>
<td>6</td>
</tr>
<tr>
<td>$V_{ON}$</td>
<td>Input ON Threshold Voltage</td>
<td>Applied between : $V_{UP1-UPC}, V_{VP1-VPC}, V_{WP1-WP}$</td>
<td>$V_{P1+VPC}$</td>
<td>1.2</td>
</tr>
<tr>
<td>$V_{OFF}$</td>
<td>Input OFF Threshold Voltage</td>
<td>$V_{ON} \cdot V_{N1-NC}$</td>
<td>$V_{P1+VPC}$</td>
<td>1.7</td>
</tr>
<tr>
<td>SC</td>
<td>Short Circuit Trip Level</td>
<td>$-20 \leq T_j \leq 125^\circ C, V_D = 15V$</td>
<td>(Fig. 3,6)</td>
<td>200</td>
</tr>
<tr>
<td>toff(SC)</td>
<td>Short Circuit Current Delay Time</td>
<td>$V_D = 15V$</td>
<td>(Fig. 3,6)</td>
<td>—</td>
</tr>
<tr>
<td>OT</td>
<td>Over Temperature Protection</td>
<td>$V_D = 15V$</td>
<td>Reset level</td>
<td>—</td>
</tr>
<tr>
<td>UV</td>
<td>Supply Circuit Under-Voltage Protection</td>
<td>$-20 \leq T_j \leq 125^\circ C$</td>
<td>Reset level</td>
<td>—</td>
</tr>
<tr>
<td>$IFO(HI)$</td>
<td>Fault Output Current</td>
<td>$V_D = 15V, V_{FO} = 15V$</td>
<td>(Note-2)</td>
<td>—</td>
</tr>
<tr>
<td>$IFO(L)$</td>
<td>Minimum Fault Output Pulse Width</td>
<td>$V_D = 15V$</td>
<td>(Note-2)</td>
<td>1.0</td>
</tr>
</tbody>
</table>

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Mounting torque</td>
<td>Main terminal screw : M5</td>
<td>2.5</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>Mounting torque</td>
<td>Mounting part screw : M5</td>
<td>2.5</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td>Weight</td>
<td>—</td>
<td>800</td>
<td>—</td>
</tr>
</tbody>
</table>

RECOMMENDED CONDITIONS FOR USE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Recommended value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply Voltage</td>
<td>Applied across P-N terminals</td>
<td>$\leq 800$</td>
<td>V</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Control Supply Voltage</td>
<td>Applied between : $V_{UP1-UPC}, V_{VP1-VPC}, V_{WP1-WP}$</td>
<td>15</td>
<td>$\pm 1.5$</td>
</tr>
<tr>
<td>$V_{CN(ON)}$</td>
<td>Input ON Voltage</td>
<td>Applied between : $V_{UP1-UPC}, V_{VP1-VPC}, V_{WP1-WP}$</td>
<td>$\leq 0.8$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CN(OFF)}$</td>
<td>Input OFF Voltage</td>
<td>$V_{ON} \cdot V_{N1-NC}$</td>
<td>$\geq 9.0$</td>
<td>—</td>
</tr>
<tr>
<td>$IP_{PWM}$</td>
<td>PWM Input Frequency</td>
<td>Using Application Circuit of Fig. 8</td>
<td>$\leq 20$</td>
<td>kHz</td>
</tr>
<tr>
<td>$t_{dead}$</td>
<td>Arm Shoot-through Blocking Time</td>
<td>For IPM’s each input signals</td>
<td>(Fig. 7)</td>
<td>$\geq 2.5$</td>
</tr>
</tbody>
</table>

(Note-3) With ripple satisfying the following conditions: $dv/dt$ swing $\leq \pm 5V/\mu s$, Variation $\leq 2V$ peak to peak
PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (Vd), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state. After this, the specified ON and OFF level setting for each input signal should be done.

2. When performing “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above Vces rating of the device. (These tests should not be done by using a curve tracer or its equivalent.)
NOTES FOR STABLE AND SAFE OPERATION:

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM’s input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: $CTR > 100\%$
- Use 4 isolated control power supplies (Vd). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.

Fig. 8 Application Example Circuit
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PERFORMANCE CURVES

OUTPUT CHARACTERISTICS
(INVERTER PART · TYPICAL)

COLLECTOR-EMITTER VOLTAGE VCE (V)

COLLECTOR CURRENT IC (A)

COLLECTOR-EMITTER SATURATION VOLTAGE VCE (sat) (V)

CONTROL SUPPLY VOLTAGE VD (V)

SWITCHING TIME tc(on), tc(off) (µs)

COLLECTOR-EMITTER SATURATION VOLTAGE (VS. Ic) CHARACTERISTICS
(INVERTER PART · TYPICAL)

OUTPUT CHARACTERISTICS
(INVERTER PART · TYPICAL)

CONTROL SUPPLY VOLTAGE VD (V)

COLLECTOR CURRENT IC (A)

SWITCHING TIME CHARACTERISTICS
(TYPICAL)

SWITCHING LOSS CHARACTERISTICS
(TYPICAL)

COLLECTOR CURRENT IC (A)

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