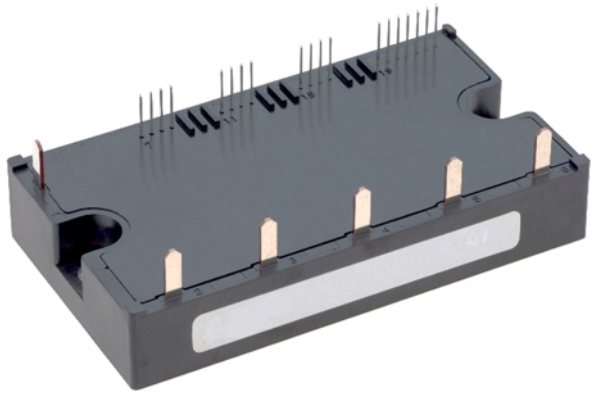
MITSUBISHI ELECTRIC

<Intelligent Power Modules>

PM50CG1AP065/PM50CG1APL065

FLAT-BASE TYPE
INSULATED PACKAGE



FEATURE

a) Adopting Full-Gate CSTBT chip.

b) The over-temperature protection which detects the chip surface temperature of CSTBT is adopted.

c) Error output signal is available from each protection upper and lower arm of IPM.

d) Outputting an error signal corresponding to the abnormal state (error mode identification)

This product is compliant with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) directive 2011/65/EU.

APPLICATION

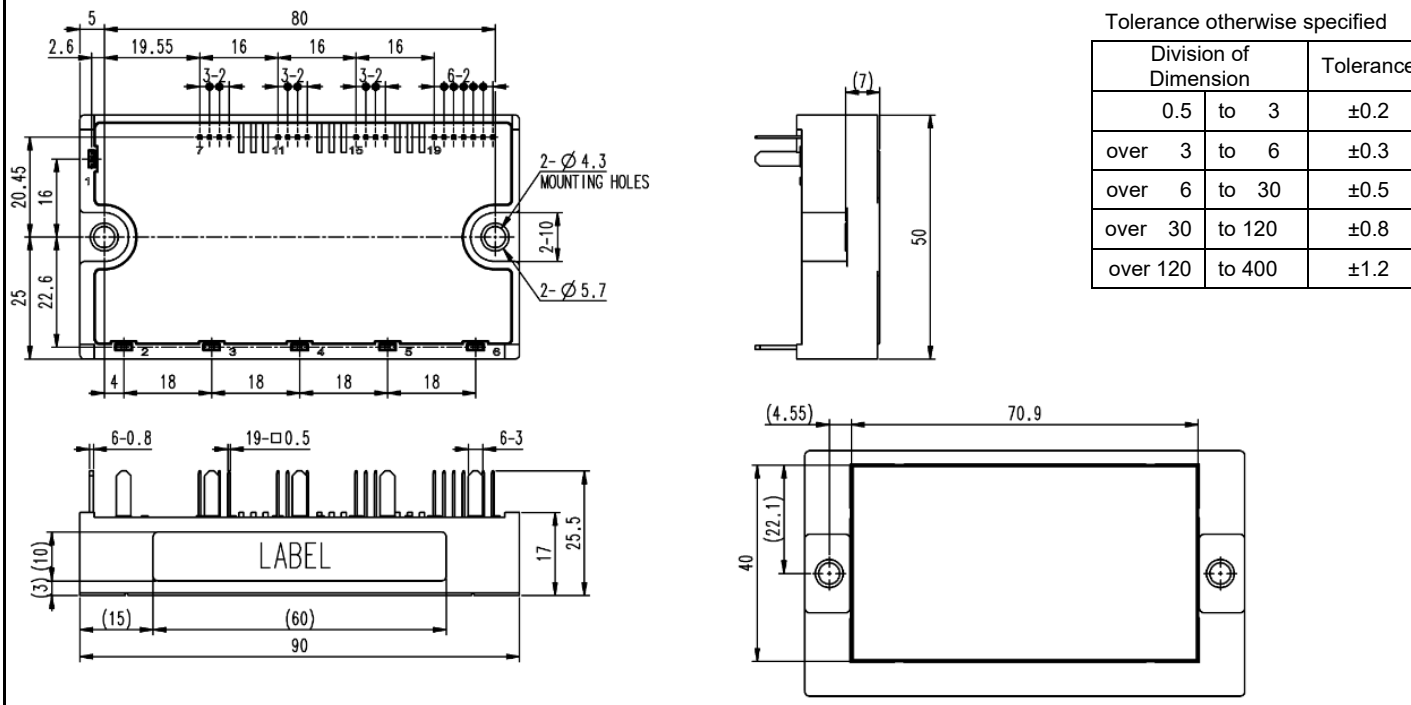
General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES

Dimensions in mm

Tolerance otherwise specified

Division of Dimension		Tolerance
0.5	to 3	±0.2
over 3	to 6	±0.3
over 6	to 30	±0.5
over 30	to 120	±0.8
over 120	to 400	±1.2



TERMINAL CODE

----CG1AP type----

1.NC, 2.P, 3.N, 4.U, 5.V, 6.W, 7.V_{UPC}, 8.U_{FO}, 9.U_P, 10.V_{UP1}, 11.V_{VPC}, 12.V_{FO}, 13.V_P, 14.V_{VP1}, 15.V_{WPC}, 16.W_{FO}, 17.W_P, 18.V_{WP1}, 19.V_{NC}, 20.V_{N1}, 21.NC, 22.U_N, 23.V_N, 24.W_N, 25.F_O

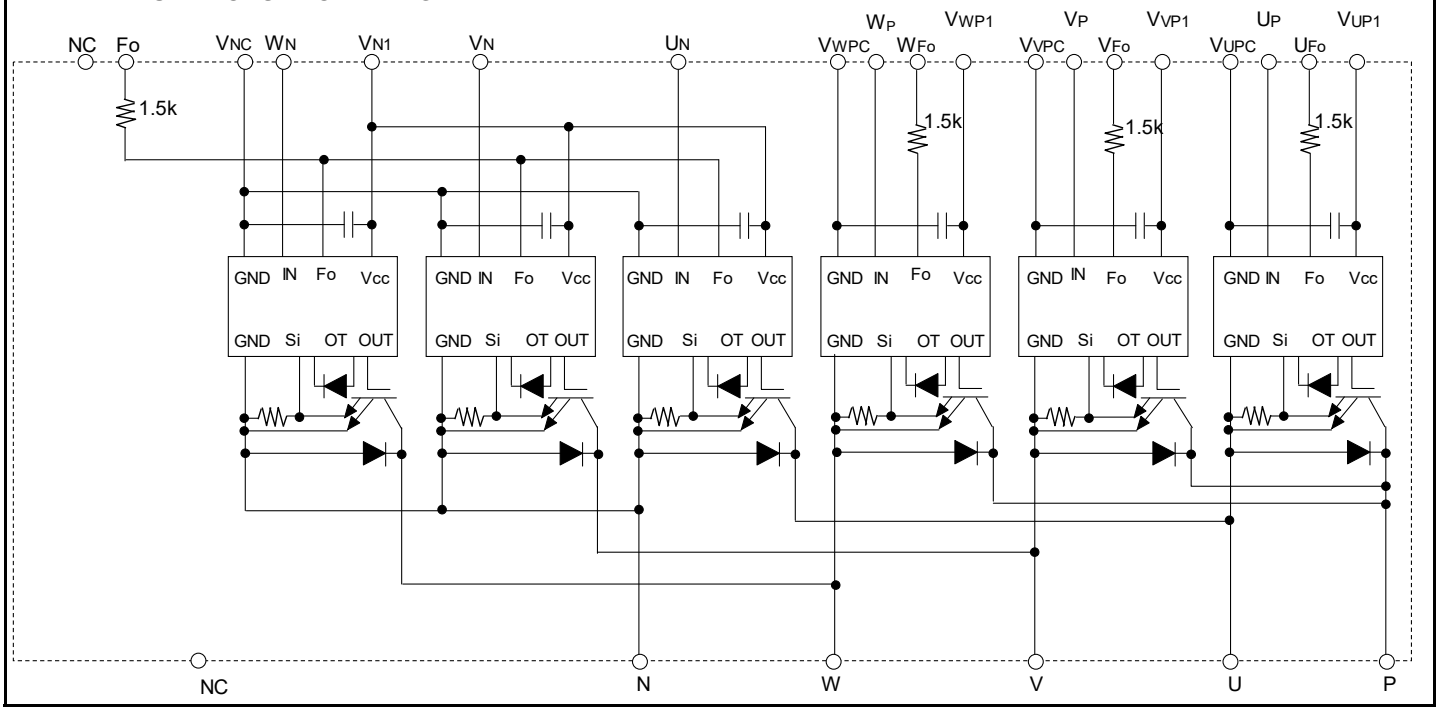
----CG1APL type----

1.N, 2.P, 3.NC, 4.U, 5.V, 6.W, 7.V_{UPC}, 8.U_{FO}, 9.U_P, 10.V_{UP1}, 11.V_{VPC}, 12.V_{FO}, 13.V_P, 14.V_{VP1}, 15.V_{WPC}, 16.W_{FO}, 17.W_P, 18.V_{WP1}, 19.V_{NC}, 20.V_{N1}, 21.NC, 22.U_N, 23.V_N, 24.W_N, 25.F_O

PM50CG1AP065/PM50CG1APL065

HIGH POWER SWITCHING USE
INSULATED TYPE

INTERNAL FUNCTIONS BLOCK DIAGRAM



MAXIMUM RATINGS (Tvj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions	Ratings	Unit
V_{CES}	Collector-Emitter Voltage	V_D=15 V, V_{CIN}=15 V	650	V
I_C	Collector Current	T_C=25 °C	50	A
I_{CRM}		Pulse	100	
P_{tot}	Total Power Dissipation	T_C=25 °C	240	W
I_E	Emitter Current	T_C=25 °C	50	A
I_{ERM}	(Free-wheeling Diode Forward current)	Pulse	100	
Tvj	Junction Temperature		-20 ~ +150	°C

*: Tc measurement point is just under the chip.

CONTROL PART

Symbol	Parameter	Conditions	Ratings	Unit
V_D	Supply Voltage	Applied between: V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	20	V
V_{CIN}	Input Voltage	Applied between: U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, U_N, V_N, W_N-V_{NC}	20	V
V_{FO}	Fault Output Supply Voltage	Applied between: U_{FO}-V_{UPC}, V_{FO}-V_{VPC}, W_{FO}-V_{WPC}, Fo-V_{NC}	20	V
I_{FO}	Fault Output Current	Sink current at U_{FO}, V_{FO}, W_{FO}, Fo terminals	20	mA

TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(PROT)}$	Supply Voltage Protected by SC	V_D =13.5 V~16.5 V, Inverter Part, Tvj=+125°C start	400	V
T_{stg}	Storage Temperature	-	-40 ~ +125	°C
T_C	Operating Case Temperature	-	-20 ~ +125	°C
V_{isol}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base plate, AC 1min, RMS	2500	V

*: Tc measurement point is just under the chip.

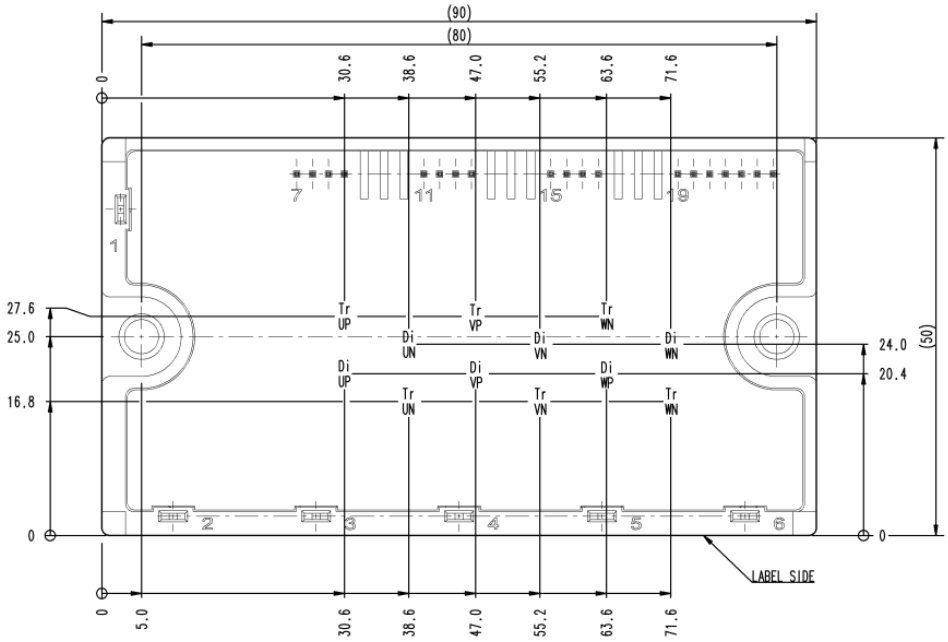
THERMAL RESISTANCE

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Thermal Resistance	Junction to case, IGBT, per 1 element (Note1)	-	-	0.52	K/W
$R_{th(j-c)D}$		Junction to case, FWD, per 1 element (Note1)	-	-	0.88	
$R_{th(c-s)}$	Contact Thermal Resistance	Case to heat sink, per 1 module, Thermal grease applied (Note.1, 2)	-	19.1	-	K/kW

Note1. If you use this value, $R_{th(s-a)}$ should be measured just under the chips.

Note2. Typical value is measured by using thermally conductive grease of λ=0.9W/(m·K), $D_{(C-S)}$=50 μm.

CHIP LOCATION (Top view) Dimension in mm, torelance: ±1mm



Tr** : IGBT
Di** : FWD

ELECTRICAL CHARACTERISTICS (Tvj= 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions			Limits			Unit
					Min.	Typ.	Max.	
V_{CEsat}	Collector-Emitter Saturation Voltage	V_D=15 V, I_C=50 A, V_{CIN}=0 V, Pulsed, (Fig.1)	Tvj=25 °C	Terminal	-	-	1.7	V
				Chip	-	1.25	-	
			Tvj=125 °C	Terminal	-	-	1.95	
				Chip	-	1.33	-	
V_{EC}	Emitter-Collector Voltage	V_D=15 V, I_E=50 A, V_{CIN}= 15 V, pulsed, (Fig.2)	Tvj=25 °C	Terminal	-	-	1.9	V
				Chip	-	1.40	-	
			Tvj=125 °C	Terminal	-	-	2.0	
				Chip	-	1.45	-	
t_{on}	Switching Time	V_D=15 V, V_{CIN}=0 V⟷15 V, V_{CC}=300 V, I_C=50A, Tvj=125 °C, Inductive Load (Fig.3, 4)			0.3	0.6	1.2	μs
t_{rr}					-	0.2	0.65	
$t_{c(on)}$					-	0.17	0.75	
t_{off}					-	1.0	2.3	
$t_{c(off)}$					-	0.13	0.4	
I_{CES}	Collector-Emitter Cut-off Current	V_{CE}=V_{CES}, V_D=15 V, V_{CIN}=15 V (Fig.5)		Tvj=25 °C	-	-	1	mA
				Tvj=125 °C	-	-	10	

ELECTRICAL CHARACTERISTICS (Tvj = 25°C, unless otherwise noted)

CONTROL PART

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit Current	V_D=15 V, V_{CIN}=15 V	V_{P1}-V_{PC}	-	4	6	mA
			V_{N1}-V_{NC}	-	12	18	
		V_D=15 V, V_{CIN}=0 V⟷15 V, V_{CC}=400 V	V_{P1}-V_{PC}	-	10	12	
		I_C=0A, Tvj=125 °C, f_C≤20kHz	V_{N1}-V_{NC}	-	29	35	
$V_{th(ON)}$	Input ON Threshold Voltage	Applied between:		1.2	1.5	1.8	V
$V_{th(OFF)}$	Input OFF Threshold Voltage	U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, U_N, V_N, W_N-V_{NC}		1.7	2.0	2.3	
SC	Short Circuit Trip Level	-20≤Tvj≤125 °C, V_D=15 V (Fig.3, 6)		100	-	-	A
$t_{d(SC)}$	Short Circuit Current Delay Time	V_D=15 V, Tvj=125 °C (Fig.3, 6)		-	2.0	-	μs
OT	Over Temperature Protection	Detect temperature of IGBT chip surface	Trip level	150	-	-	°C
$OT_{(hys)}$			Hysteresis	-	20	-	
UV_t	Supply Circuit Under-Voltage Protection	-	Trip level	11.0	12.0	12.7	V
UV_r			Reset level	-	12.5	-	
$I_{FO(H)}$	Fault Output Current	V_D=15 V, V_{FO}=15 V (Note3)		-	-	0.01	mA
$I_{FO(L)}$				-	10	15	
t_{FO}	Fault Output Pulse Width	V_D=15 V (Note3)	OT	-	8.0	-	ms
			UV	-	4.0	-	
			SC	-	2.0	-	

Note3. Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
M_s	Mounting Torque	Mounting part screw : M4	1.5	1.7	2.0	N•m
m	mass	-	-	175	-	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Conditions	Recommended value	Unit
V_{CC}	Supply Voltage	Applied across P-N terminals	≤ 400	V
V_D	Control Supply Voltage	Applied between : V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC} (Note4)	15.0±1.5	V
$V_{CIN(ON)}$	Input ON Voltage	Applied between : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}, U_N, V_N, W_N-V_{NC}	≤ 0.8	V
$V_{CIN(OFF)}$	Input OFF Voltage		≥ 9.0	
f_{PWM}	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
t_{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig.7)	≥ 2.0	μs

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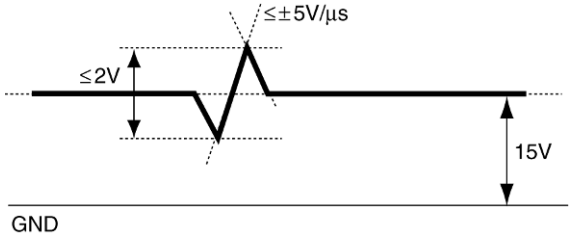
Note4. With ripple satisfying the following conditions: dv/dt swing ≤ ±5 V/μs, Variation ≤ 2 V peak to peak



PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
   After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
   (These test should not be done by using a curve tracer or its equivalent.)

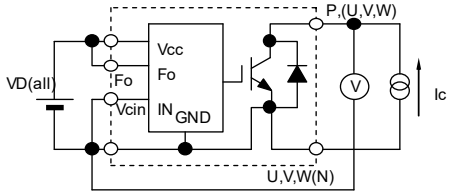


Fig.1 V_{CEsat} Test

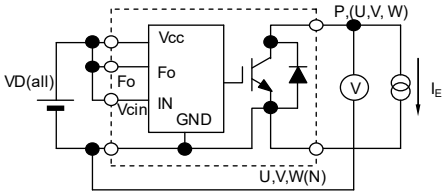


Fig.2 V_{EC} Test

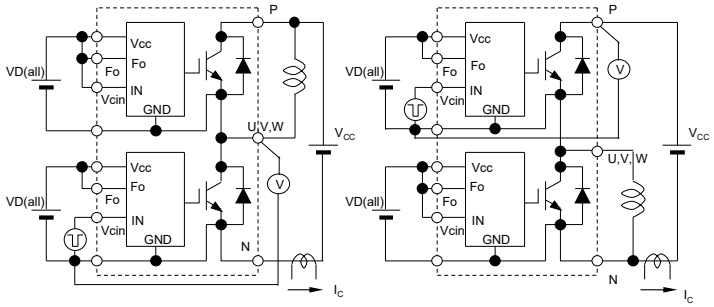


Fig.3 Switching time and SC test circuit

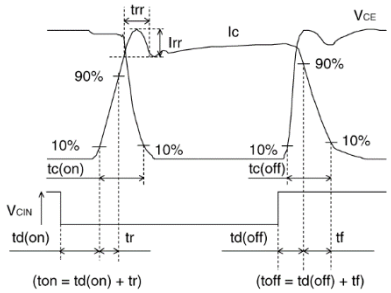


Fig.4 Switching time test waveform

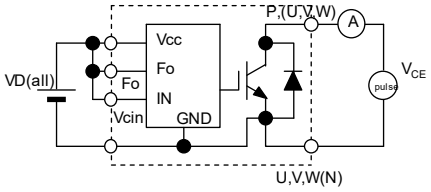


Fig.5 I_{CES} Test

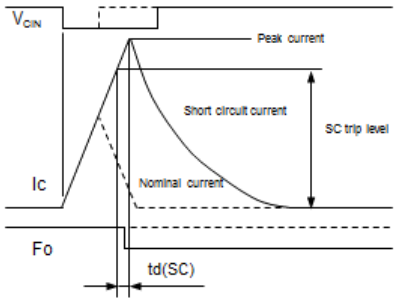
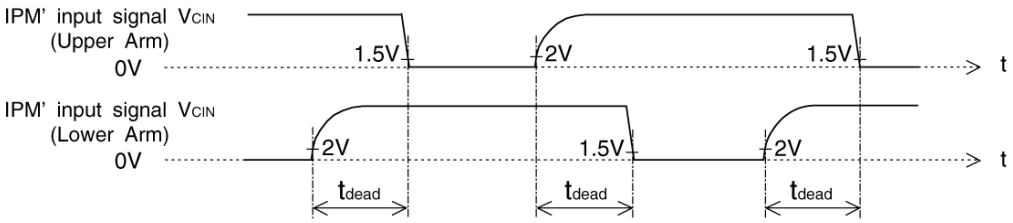


Fig.6 SC test waveform



1.5V: Input on threshold voltage Vth(on) typical value, 2V: Input off threshold voltage Vth(off) typical value

Fig. 7 Dead time measurement point example

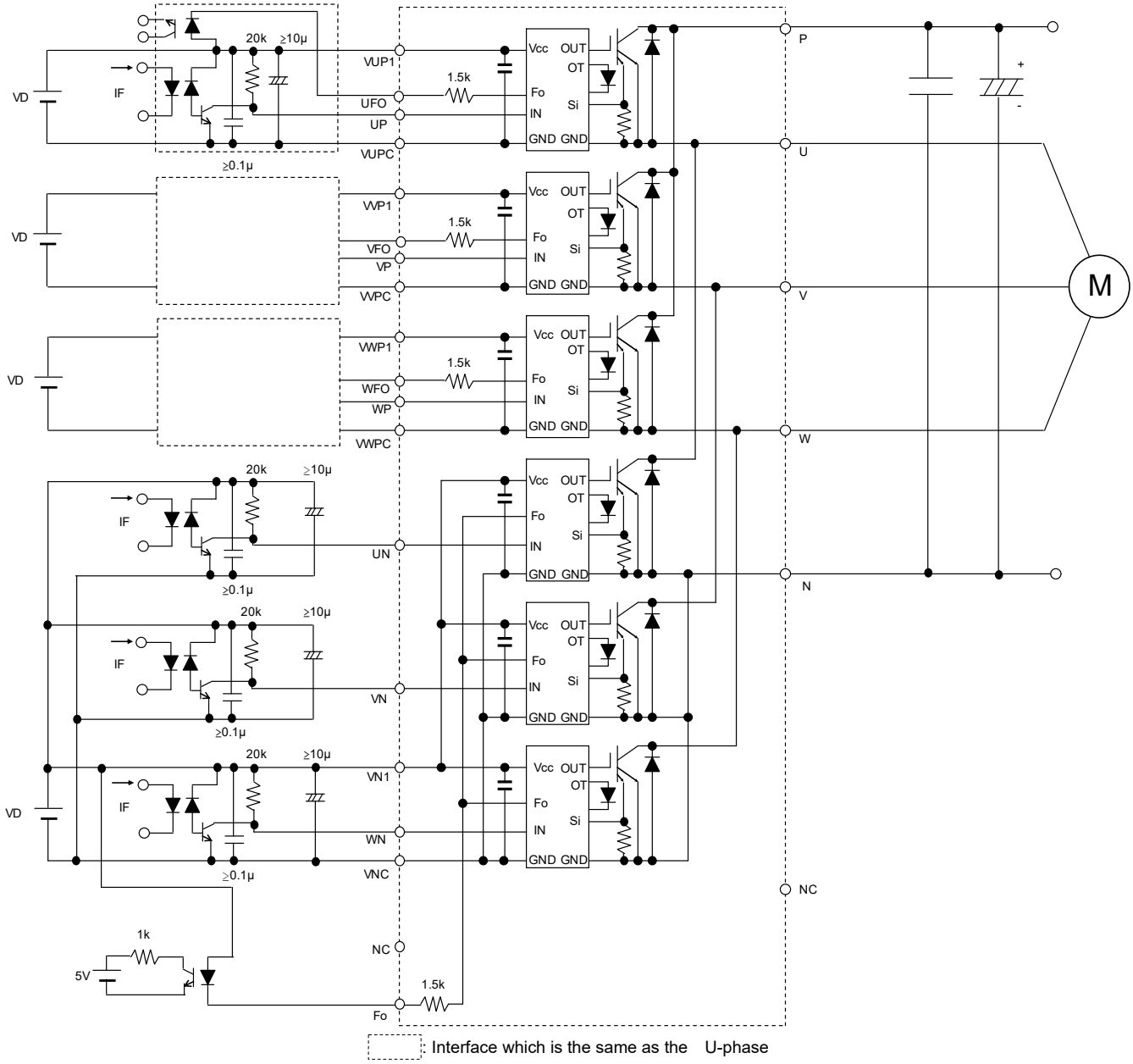


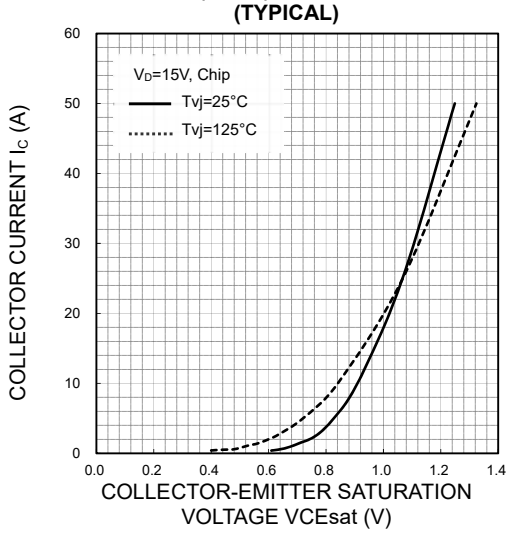
Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

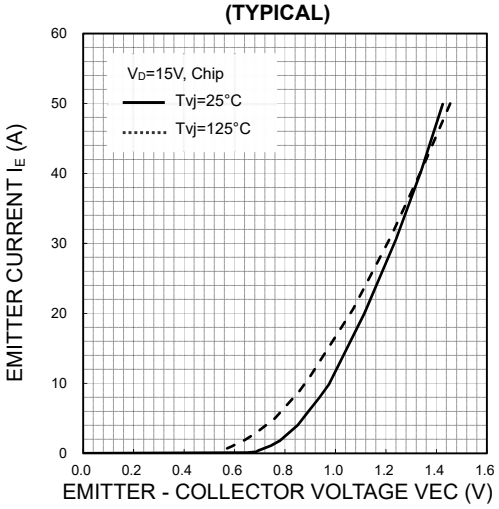
- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: t_{PLH}, t_{PHL} ≤ 0.8μs, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.

PERFORMANCE CURVES

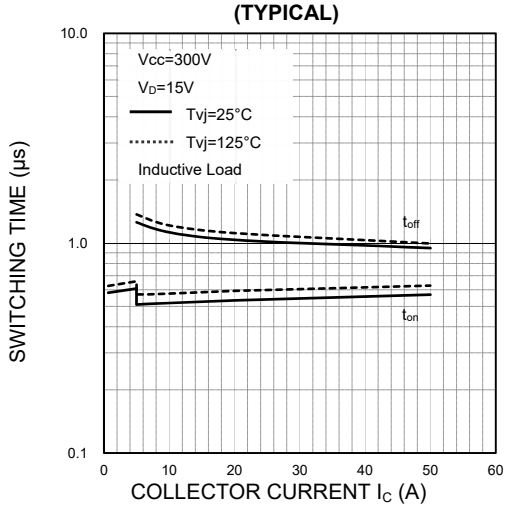
COLLECTOR-EMITTER SATURATION VOLTAGE (VS. Ic) CHARACTERISTICS (TYPICAL)



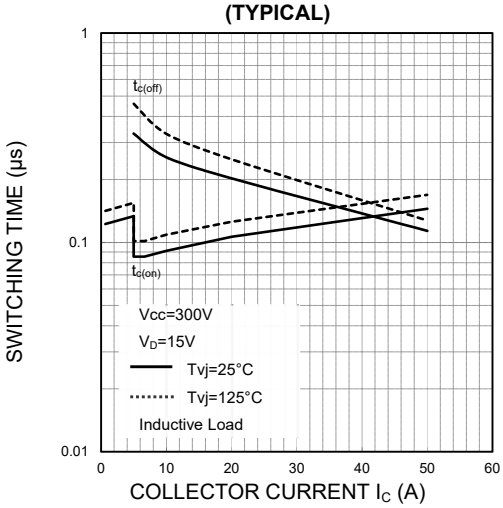
FREE WHEELING DIODE FORWARD CHARACTERISTICS (TYPICAL)



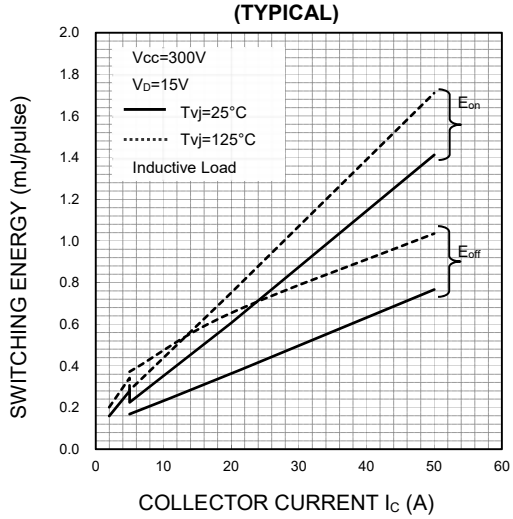
SWITCHING TIME (t_{on}, t_{off}) CHARACTERISTICS (TYPICAL)



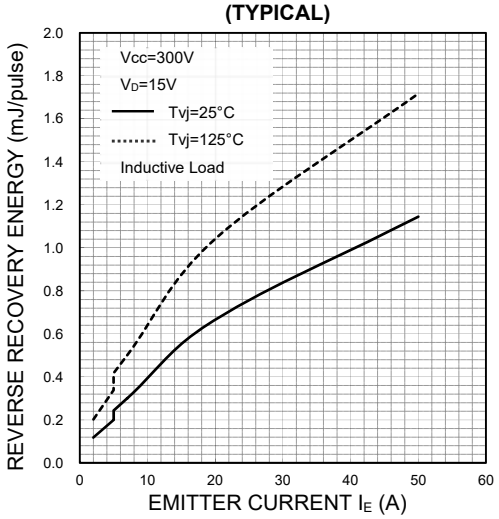
SWITCHING TIME ($t_{c(on)}$, $t_{c(off)}$) CHARACTERISTICS (TYPICAL)



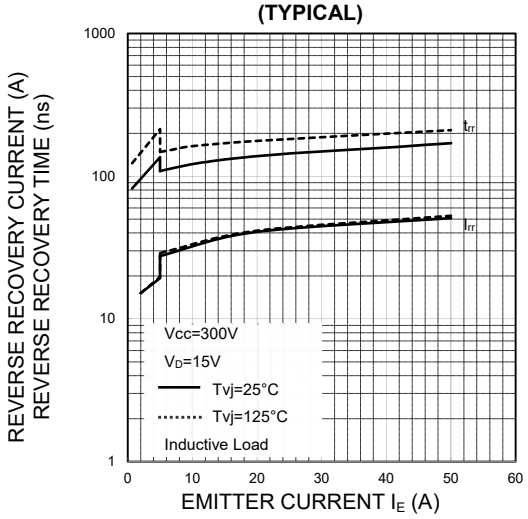
SWITCHING ENERGY CHARACTERISTICS (TYPICAL)



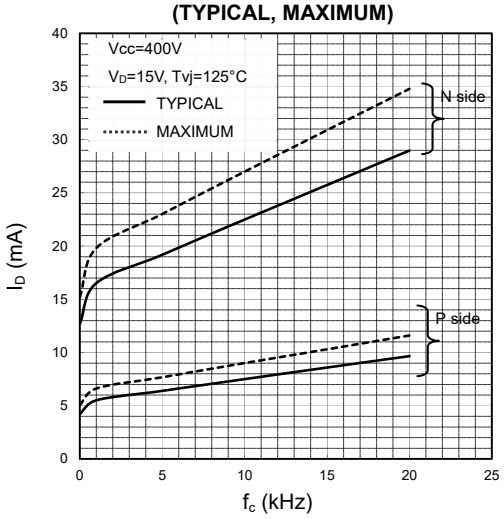
FREE WHEELING DIODE REVERSE RECOVERY ENERGY CHARACTERISTICS (TYPICAL)



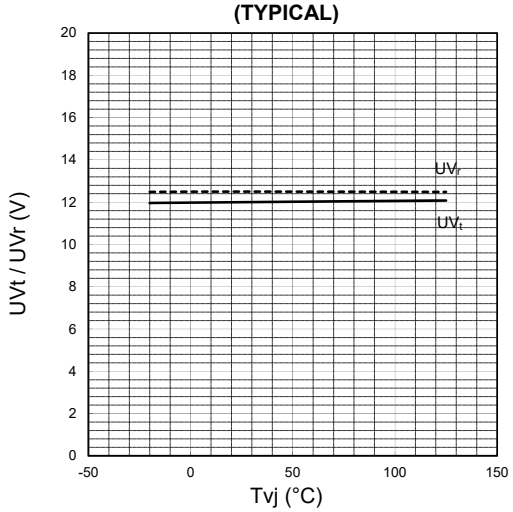
FREE WHEELING DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)



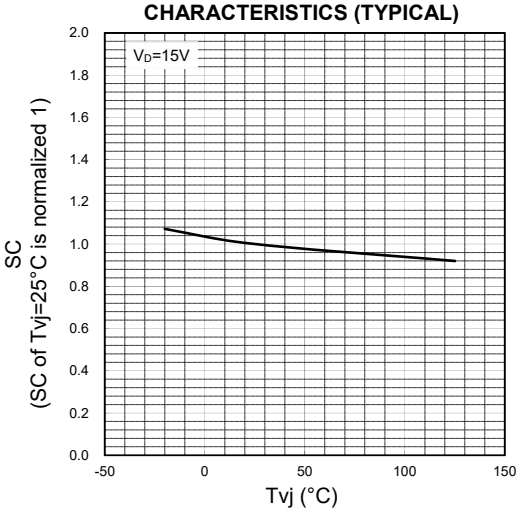
I_D VS. f_C CHARACTERISTICS (TYPICAL, MAXIMUM)



UV TRIP LEVEL VS. Tvj CHARACTERISTICS (TYPICAL)

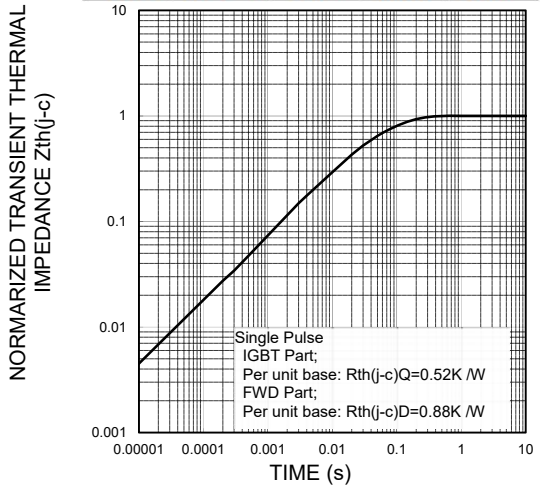


SC TRIP LEVEL VS. Tvj CHARACTERISTICS (TYPICAL)



TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (TYPICAL)

i	1	2	3	4
Ri	0.0124	0.0739	0.3505	0.5632
τ i (s)	1.961E-05	0.0014	0.0179	0.0944



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