

TENTATIVE

PS21069

Transfer-Mold Type
Insulated Type

Pre.	S.Kaw, M. Sakai, T. Inagaki	Rev.	A
Apr.	T. Gotohda 30 Nov. '04		

Applications : AC100~200V three-phase motor variable speed inverter drive.

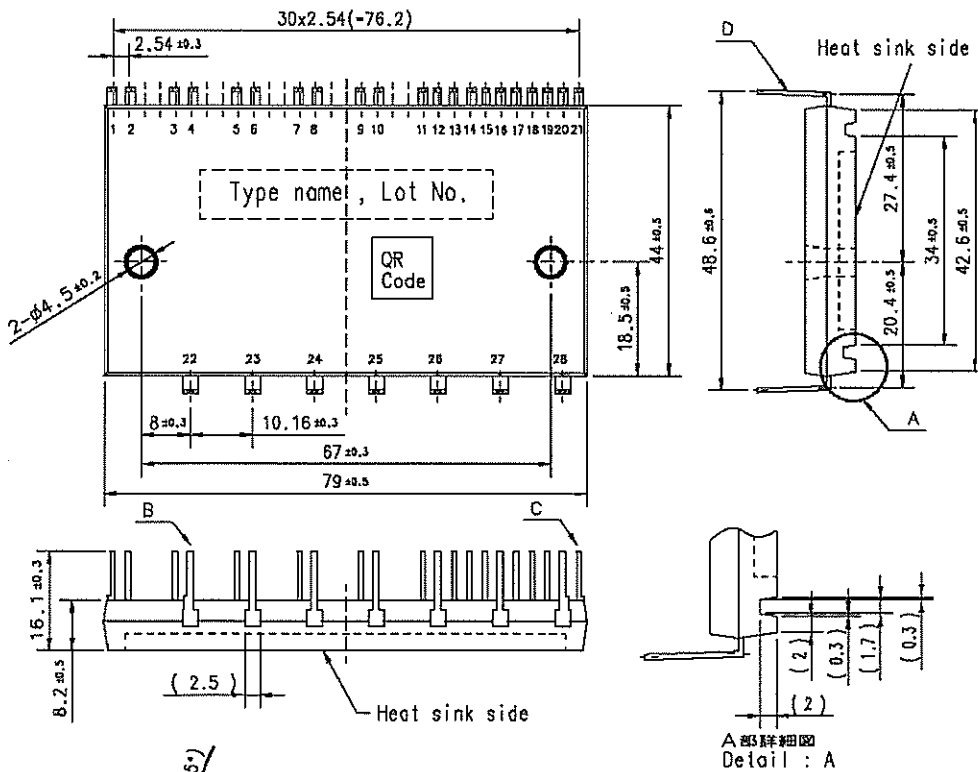
Integrated Power Functions :

600V/50A low-loss 5th generation IGBT (CSTBT™) inverter bridge with N-side open emitter structure for DC-to-AC power conversion

Integrated drive, protection and system control functions :

- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to an SC fault (Lower-side IGBT) or a UV fault (Lower-side supply).
- Input interface : 5V line CMOS/TTL compatible, Schmitt Trigger receiver circuit (High Active).

Fig. 1 Package Outlines



Note 1: Package outlines are subjected to change in the development.
 Note 2: All lead terminals are treated by Pb-free solder (ingredient: Sn-Cu) plating.

TENTATIVE**PS21069**Transfer-Mold Type
Insulated TypeMaximum Ratings ($T_j=25^\circ\text{C}$, unless otherwise noted):

Inverter Part:

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}	Applied between P-NU,NV,NW	450	V
Supply voltage (surge)	$V_{CC(surge)}$	Applied between P-NU,NV,NW	500	V
Collector-emitter voltage	V_{CES}		600	V
Each IGBT collector current	$\pm I_C$	$T_c=25^\circ\text{C}$	50	A
Each IGBT collector current (peak)	$\pm I_{CP}$	$T_c=25^\circ\text{C}$, less than 1ms	100	A
Collector dissipation	P_C	$T_c=25^\circ\text{C}$, per 1 chip	70.4	W
Junction temperature	T_j	(Note 1)	-20~+125	$^\circ\text{C}$

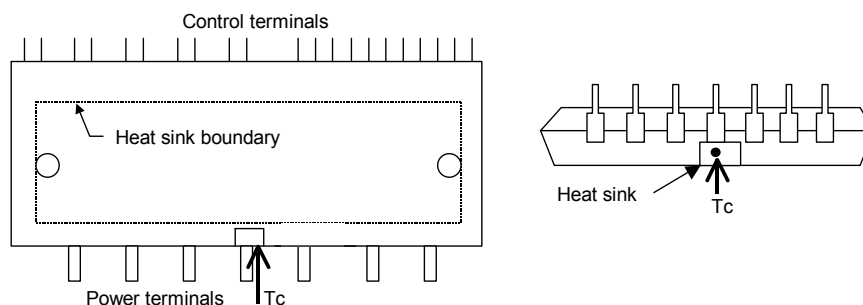
(Note 1) The maximum junction temperature rating of the power chips integrated within the DIP-IPM is $150^\circ\text{C} (@T_c \leq 100^\circ\text{C})$. However, in order to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq 125^\circ\text{C} (@T_c \leq 100^\circ\text{C})$.

Control (Protection) Part

Item	Symbol	Condition	Rating	Unit
Control supply voltage	V_D	Applied between $V_{P1}-V_{PC}, V_{N1}-V_{NC}$	20	V
Control supply voltage	V_{DB}	Applied between $V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}$	20	V
Input voltage	V_{IN}	Applied between $U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}$	-0.5~ $V_D+0.5$	V
Fault output supply voltage	V_{FO}	Applied between Fo- V_{NC}	-0.5~ $V_D+0.5$	V
Fault output current	I_{FO}	Sink current at Fo terminal	1	mA
Current sensing input voltage	V_{SC}	Applied between CIN- V_{NC}	-0.5~ $V_D+0.5$	V

Total System

Item	Symbol	Condition	Rating	Unit
Self protection supply voltage limit (short circuit protection capability)	$V_{CC(prot)}$	$V_D=13.5\sim 16.5\text{V}$, Inverter part $T_j=125^\circ\text{C}$, non-repetitive less than 2 μs	400	V
Module case operation temperature	T_c	(Note 2)	-20~+100	$^\circ\text{C}$
Storage temperature	T_{stg}		-40~+125	$^\circ\text{C}$
Isolation voltage	Viso	60Hz, Sinusoidal, AC 1 minutes, connection pins to heat-sink plate	2500	Vrms

(Note 2) T_c measurement position

DIP-IPM	DPH-3920e-	
---------	------------	--

TENTATIVE**PS21069**Transfer-Mold Type
Insulated Type

Thermal Resistance :

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case thermal resistance	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6 module)	—	—	1.42	°C / W
	$R_{th(j-c)F}$	Inverter FWD part (per 1/6 module)	—	—	2.30	
Contact thermal resistance (Note 3)	$R_{th(c-f)}$	Between case and fin with grease applied (per 1 module)	—	—	0.047	

(Note 3) Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100 μ m~+200 μ m on the contacting surface of DIP-IPM and heat-sink.

Electrical Characteristics ($T_j=25^\circ\text{C}$, unless otherwise noted) :

Inverter Part

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_D=V_{DB}=15\text{V}$ $V_{IN}=5\text{V}$, $I_C=50\text{A}$,	$T_j=25^\circ\text{C}$	—	1.50	2.00	V
			$T_j=125^\circ\text{C}$	—	1.60	2.10	
FWD forward voltage	V_{EC}	$T_j=25^\circ\text{C}$, $V_{IN}=0\text{V}$, $-I_C=50\text{A}$	—	1.70	2.20	V	
Switching time	t_{on}	$V_{CC}=300\text{V}$, $V_D=V_{DB}=15\text{V}$ $V_{IN}=5\leftrightarrow 0\text{V}$, $I_C=50\text{A}$	—	0.70	1.30	1.90	μs
	t_{rr}		—	0.30	—		
	$t_{c(on)}$	$T_j=125^\circ\text{C}$	—	0.40	0.60		
	t_{off}	Inductive load (upper-lower arm)	—	2.00	2.60		
	$t_{c(off)}$		—	0.65	0.90		
Collector-emitter cut-off current	I_{CES}	$V_{CE}=V_{CES}$	$T_j=25^\circ\text{C}$	—	—	1	mA
			$T_j=125^\circ\text{C}$	—	—	10	

Control (Protection) Part :

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Circuit current	I_D	$V_D=V_{DB}=15\text{V}$ $V_{IN}=5\text{V}$	Total of $V_{P1}-V_{PC}$, $V_{N1}-V_{NC}$	—	—	7.00	mA
			$V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	—	—	0.55	
		$V_D=V_{DB}=15\text{V}$ $V_{IN}=0\text{V}$	Total of $V_{P1}-V_{PC}$, $V_{N1}-V_{NC}$	—	—	7.00	
			$V_{UFB}-V_{UFS}$, $V_{VFB}-V_{VFS}$, $V_{WFB}-V_{WFS}$	—	—	0.55	
Fo output voltage	V_{FOH}	$V_{sc}=0\text{V}$, Fo circuit:10k Ω to 5V pull-up	4.9	—	—	V	
	V_{FOL}	$V_{sc}=1\text{V}$, $I_{FO}=1\text{mA}$	—	—	0.95		
Input current	I_{IN}	$V_{IN}=5\text{V}$	1.0	1.5	2.0	mA	
short circuit trip level	$V_{SC(ref)}$	$T_j=25^\circ\text{C}$, $V_D=15\text{V}$ (Note 4)	0.43	0.48	0.53	V	
Control supply under-voltage protection	UV_{DBt}	$T_j \leq 125^\circ\text{C}$	Trip level	10.0	—	12.0	V
	UV_{DBr}		Reset level	10.5	—	12.5	
	UV_{Dt}		Trip level	10.3	—	12.5	
	UV_{Dr}		Reset level	10.8	—	13.0	
Fault output pulse width	t_{FO}	$C_{FO}=22\text{nF}$ (Note 5)	1.0	1.8	—	ms	
ON threshold voltage	$V_{th(on)}$	Applied between U_P , V_P , W_P-V_{PC} ,	2.1	2.3	2.6	V	
OFF threshold voltage	$V_{th(off)}$	U_N , V_N , W_N-V_{NC}	0.8	1.4	2.1		

(Note 4) Short circuit protection functions only for N-side IGBTs. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the rated current.

(Note 5) Fault signal is output when the lower arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} ($C_{FO} = 12.2 \times 10^{-6} \times t_{FO} [\text{F}]$)

TENTATIVE

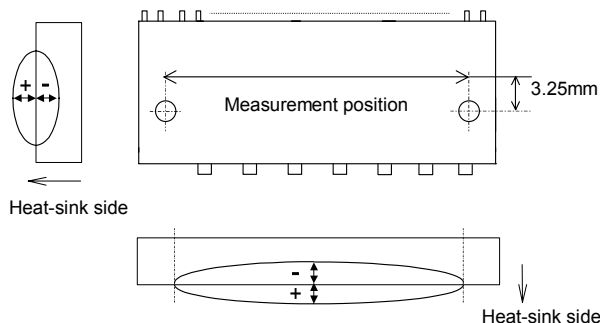
PS21069

Transfer-Mold Type
Insulated Type

Mechanical Characteristics and Ratings:

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: (M4)	Recommended: 1.18N·m	0.98	–	1.47	N·m
Weight			–	77	–	g
Heat-sink flatness	(Note7)		–50	–	100	μm

(Note7)



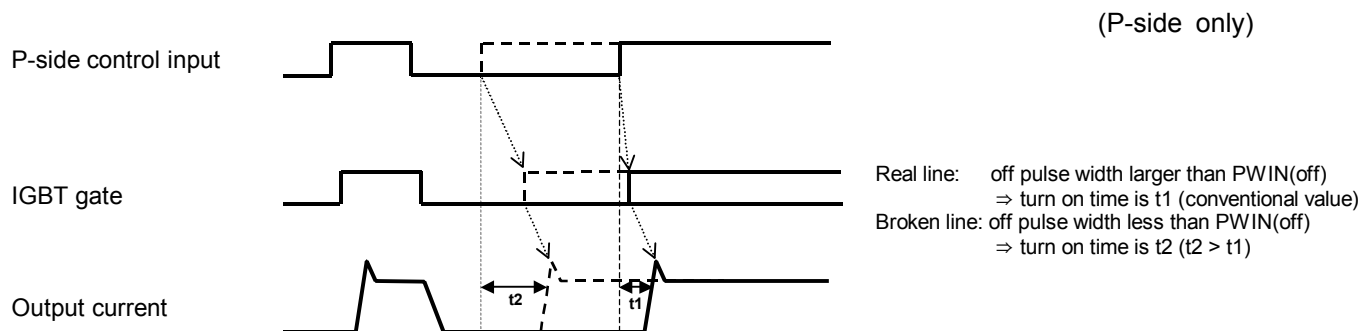
Recommended Operation Conditions :

Item	Symbol	Condition	Recommended			Unit	
			Min.	Typ.	Max.		
Supply voltage	V_{CC}	Applied between P-NU,NV,NW	0	300	400	V	
Control supply voltage	V_D	Applied between V_{P1} - V_{PC} , V_{N1} - V_{NC}	13.5	15.0	16.5	V	
Control supply voltage	V_{DB}	Applied between V_{UFB} - V_{UFS} , V_{VFB} - V_{VFS} , V_{WFB} - V_{WFS}	13.0	15.0	18.5	V	
Control supply variation	$\Delta V_D, \Delta V_{DB}$		-1	–	+1	V/μs	
Arm-shoot-through blocking time	t_{dead}	For each input signal, $T_c \leq 100^\circ C$	2.0	–	–	μs	
PWM input frequency	f_{PWM}	$T_c \leq 100^\circ C$, $T_j \leq 125^\circ C$	–	–	20	kHz	
Minimum input pulse width	PWIN(on)	(Note 7)	0.3	–	–	μs	
	PWIN(off)	200 ≤ V_{CC} ≤ 350V, 13.5 ≤ V_D ≤ 16.5V, 13.0 ≤ V_{DB} ≤ 18.5V, -20 ≤ T_f ≤ 100°C, N line wiring inductance less than 10nH (Note 8)	$I_C \leq 50A$	3.0	–		–
			$50 < I_C \leq 85A$	5.0	–		–
V_{NC} variation	V_{NC}	Potential difference between V_{NC} -NU,NV,NW including surge voltage	-5.0	–	+5.0	V	

(Note 7) DIP-IPM might make no response to the input on signal with pulse width less than PWIN(on).

(Note 8) DIP-IPM might make no response to the input off signal with pulse width less than PWIN(off), or P-side only the turn on time becomes long as shown in Fig.2. However, off-latch will not happen for next input on signal in this case. For the wiring inductance of N line, please refer to Fig.6.

Fig.2 Output behavior under short input off signal with pulse width less than PWIN(off)



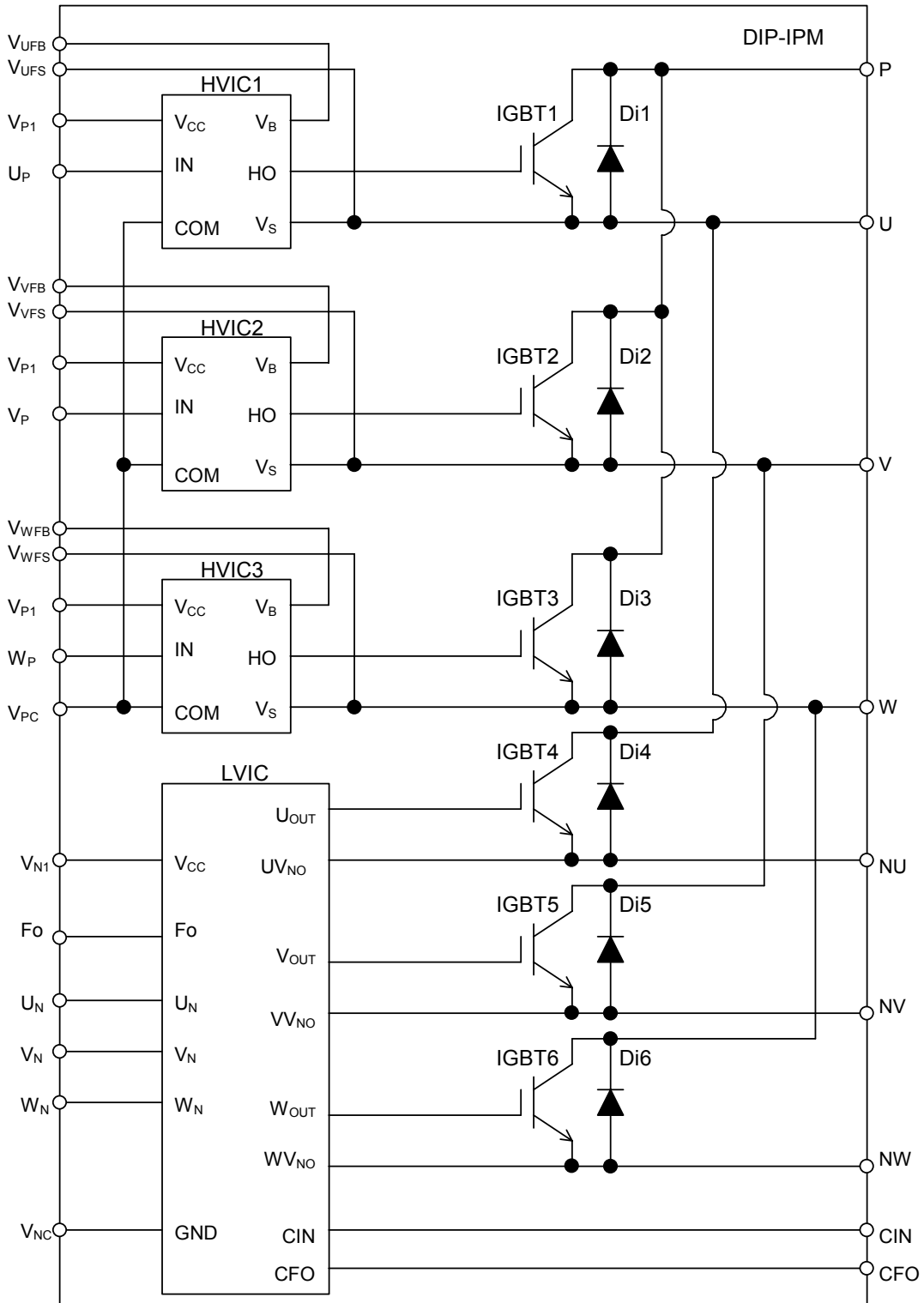
DIP-IPM	DPH-3920e-	
---------	------------	--

TENTATIVE

PS21069

Transfer-Mold Type
Insulated Type

Fig.3 DIP-IPM Internal Circuit



TENTATIVE

PS21069

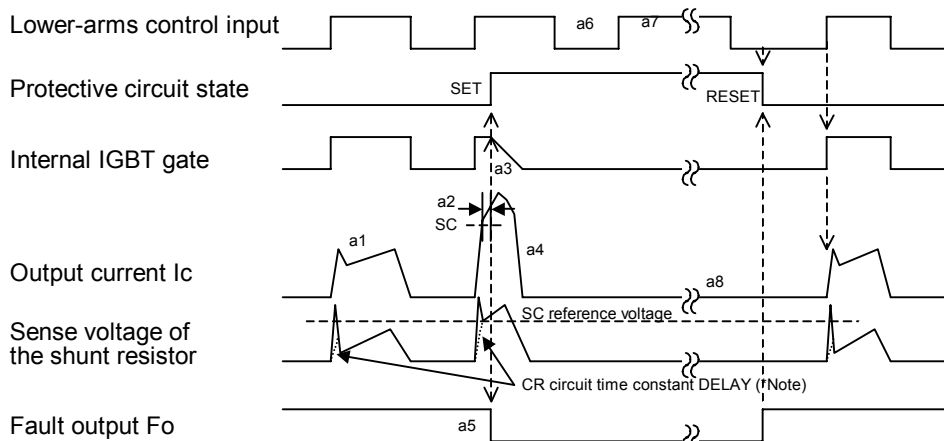
Transfer-Mold Type
Insulated Type

Fig.4 Timing Charts of the DIP-IPM Protective Functions

[A] Short-Circuit Protection (N-side only)

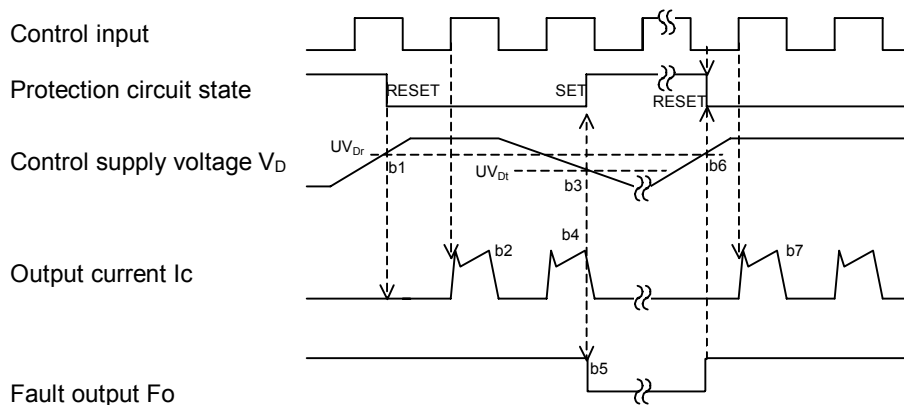
(with external shunt resistor and CR filter)

- a1. Normal operation: IGBT turn on and carry current.
- a2. Short circuit current detected (SC trigger).
- a3. IGBT gate hard interrupted.
- a4. IGBT turn off.
- a5. Fo output: Fo output pulse width is determined by the external capacitance C_{FO} .
- a6. Input "L" : IGBT off.
- a7. Input "H" : IGBT on, but during the Fo output period the IGBT will not turn ON.
- a8. IGBT keep in off state.



[B] Under- Voltage Protection (N-side, UV_D)

- b1. Control supply voltage rise: After the voltage level reaches UV_{Dr} , the drive circuit begins to work at the rising edge of the next input signal.
- b2. Normal operation: IGBT turn on and carry current.
- b3. Under voltage trip (UV_{Dt}).
- b4. IGBT turn off regardless of the control input level.
- b5. Fo output.
- b6. Under voltage reset (UV_{Dr}).
- b7. Normal operation: IGBT turn on and carry current.



TENTATIVE

PS21069

Transfer-Mold Type
Insulated Type

[C] Under- Voltage Protection (P-side, UV_{DB})

- c1. Control supply voltage rise: After the voltage reaches UV_{DBr} , the drive circuit begins to work.
- c2. Normal operation: IGBT turn on and carry current.
- c3. Under voltage trip (UV_{DBt}).
- c4. IGBT turn off regardless of the control input level, but there is no Fo signal output.
- c5. Under voltage reset (UV_{DBr}).
- c6. Normal operation: IGBT turn on and carry current.

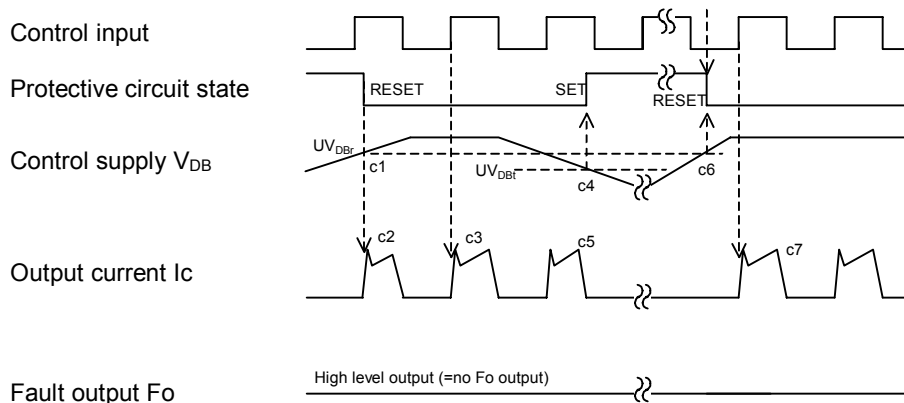
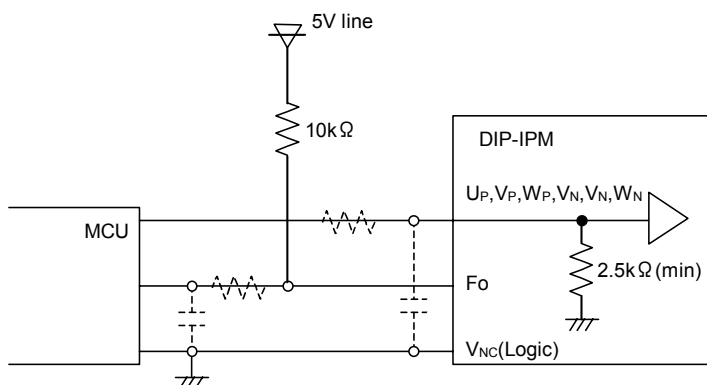


Fig.5 Recommended MCU I/O interface circuit



Note) RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The DIP-IPM input signal section integrates a 2.5kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, care must be taken to satisfy the turn-on threshold voltage requirement.

Fig.6 Wiring method of shunt resistor circuit

