# PS21246-E

**TRANSFER-MOLD TYPE**
**INSULATED TYPE**

## PS21246-E

### INTEGRATED POWER FUNCTIONS

4th generation (planar) IGBT inverter bridge for 3 phase DC-to-AC power conversion.

### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

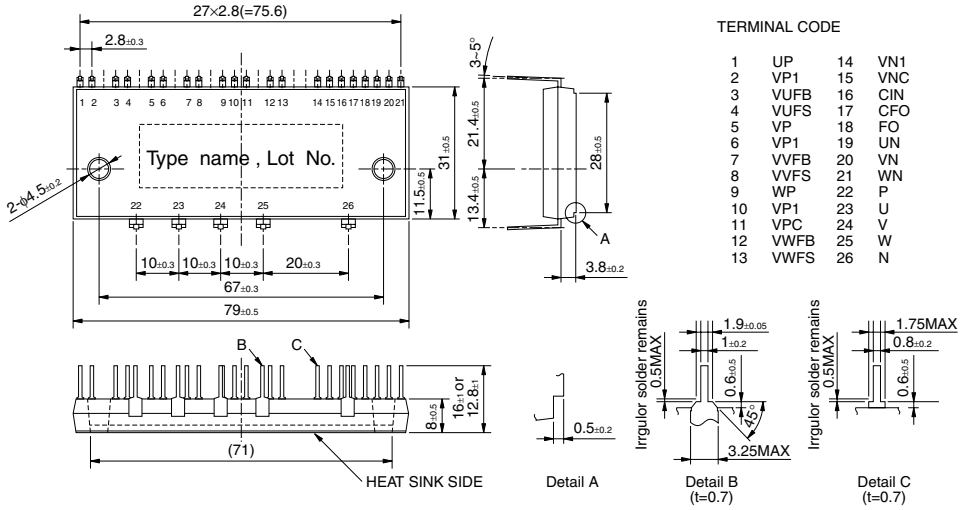
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage (UV) protection.
  Note : Bootstrap supply scheme can be applied.
- For lower-leg IGBTs : Drive circuit, Control circuit under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to a SC fault (Low-side IGBT) or a UV fault (Low-side supply).
- Input interface : 5V line CMOS/TTL compatible, Schmitt Trigger receiver circuit.

## APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

**Fig. 1 PACKAGE OUTLINES**

Dimensions in mm



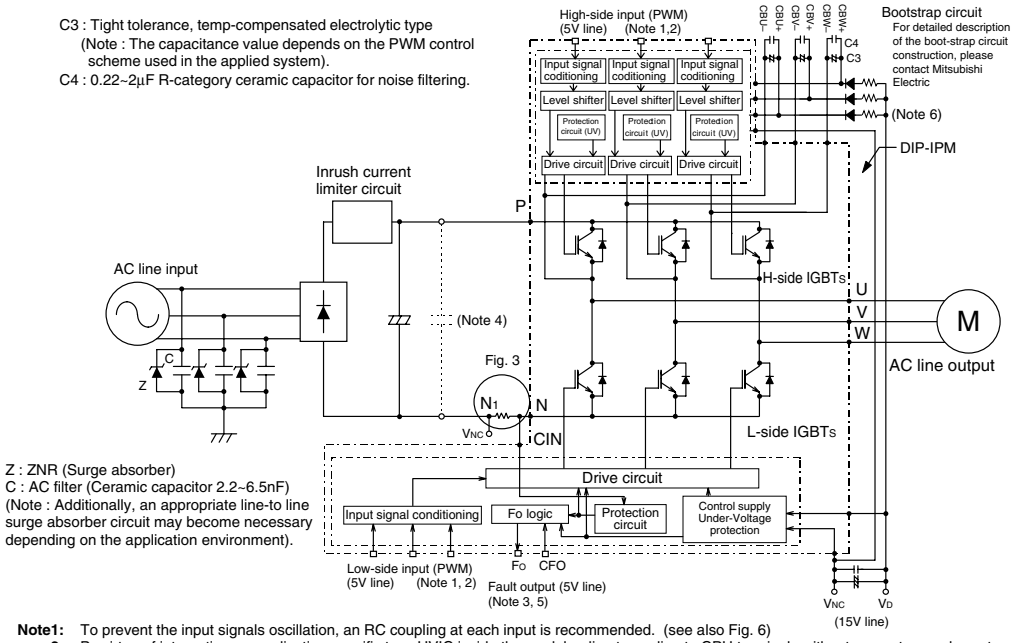

TERMINAL CODE

| | | | |
|---|---|---|---|
| 1 | UP | 14 | VN1 |
| 2 | VP1 | 15 | VNC |
| 3 | VUFB | 16 | CIN |
| 4 | VUFS | 17 | CFO |
| 5 | VP | 18 | FO |
| 6 | VP1 | 19 | UN |
| 7 | VVFB | 20 | VN |
| 8 | VVFS | 21 | WN |
| 9 | WP | 22 | P |
| 10 | VP1 | 23 | U |
| 11 | VPC | 24 | V |
| 12 | VWFB | 25 | W |
| 13 | VWFS | 26 | N |



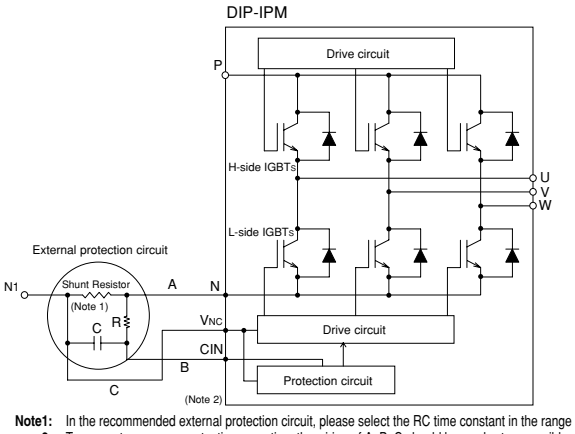
MITSUBISHI ELECTRIC

## Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

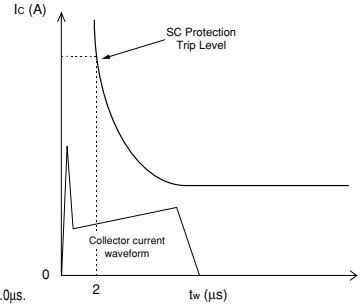



**Note1:** To prevent the input signals oscillation, an RC coupling at each input is recommended. (see also Fig. 6)
**2:** By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 6)
**3:** This output is open collector type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1kΩ resistance. (see also Fig. 6)
**4:** The wiring between the power DC link capacitor and the P/N1 terminals should be as short as possible to protect the DIP-IPM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1~0.22μF, high voltage type) is recommended to be mounted close to these P and N1 DC power input pins.
**5:** Fo output pulse width should be decided by putting external capacitor between CFO and $V_{NC}$ terminals. (Example : CFO=22nF → $t_{FO}$=1.8ms (Typ.))
**6:** High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.

## Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT




Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) after allowing a suitable filtering time (defined by the RC circuit). When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output. Since the SC fault may be repetitive, it is recommended to stop the system when the Fo signal is received and check the fault.




**Note1:** In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0μs.
**2:** To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.

**MAXIMUM RATINGS** ($T_j$ = 25°C, unless otherwise noted)

**INVERTER PART**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Applied between P-N | 450 | V |
| $V_{CC(surge)}$ | Supply voltage (surge) | Applied between P-N | 500 | V |
| $V_{CES}$ | Collector-emitter voltage | | 600 | V |
| ±$I_C$ | Each IGBT collector current | $T_C$ = 25°C | 25 | A |
| ±$I_{CP}$ | Each IGBT collector current (peak) | $T_C$ = 25°C, instantaneous value (pulse) | 50 | A |
| $P_C$ | Collector dissipation | $T_C$ = 25°C, per 1 chip | 59.5 | W |
| $T_j$ | Junction temperature | (Note 1) | –20~+150 | °C |

**Note 1** : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_C \leq 100$°C) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq 125$°C (@ $T_C \leq 100$°C).

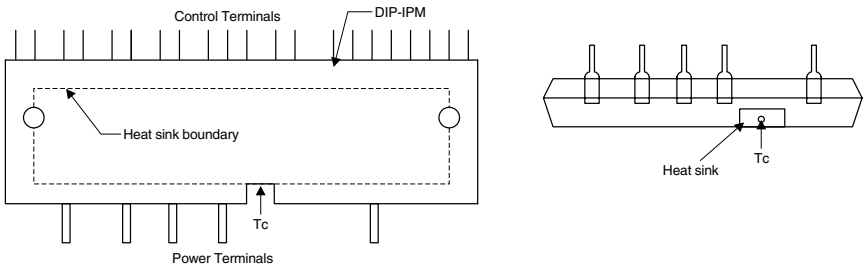
**CONTROL (PROTECTION) PART**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_D$ | Control supply voltage | Applied between $V_{P1}$-$V_{PC}$, $V_{N1}$-$V_{NC}$ | 20 | V |
| $V_{DB}$ | Control supply voltage | Applied between $V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$, $V_{WFB}$-$V_{WFS}$ | 20 | V |
| $V_{CIN}$ | Input voltage | Applied between $U_P$, $V_P$, $W_P$-$V_{PC}$, $U_N$, $V_N$, $W_N$-$V_{NC}$ | –0.5~+5.5 | V |
| $V_{FO}$ | Fault output supply voltage | Applied between $F_O$-$V_{NC}$ | –0.5~$V_D$+0.5 | V |
| $I_{FO}$ | Fault output current | Sink current at $F_O$ terminal | 15 | mA |
| $V_{SC}$ | Current sensing input voltage | Applied between CIN-$V_{NC}$ | –0.5~$V_D$+0.5 | V |

**TOTAL SYSTEM**

| Symbol | Parameter | Condition | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC(PROT)}$ | Self protection supply voltage limit (short circuit protection capability) | $V_D$ = 13.5~16.5V, Inverter part<br>$T_j$ = 125°C, non-repetitive, less than 2 µs | 400 | V |
| $T_C$ | Module case operation temperature | (Note 2) | –20~+100 | °C |
| $T_{stg}$ | Storage temperature | | –40~+125 | °C |
| $V_{iso}$ | Isolation voltage | 60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate | 1500 | $V_{rms}$ |

**Note 2 : $T_C$ MEASUREMENT POINT**



## THERMAL RESISTANCE

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $R_{th(j-c)Q}$ | Junction to case thermal resistance | Inverter IGBT part (per 1/6 module) | — | — | 2.1 | °C/W |
| $R_{th(j-c)F}$ | | Inverter FWD part (per 1/6 module) | — | — | 3.0 | °C/W |
| $R_{th(c-f)}$ | Contact thermal resistance | Case to fin, (per 1 module) thermal grease applied | — | — | 0.067 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_j$ = 25°C, unless otherwise noted)

### INVERTER PART

| Symbol | Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_D = V_{DB}$ = 15V, $V_{CIN}$ = 0V | $I_C$ = 25A, $T_j$ = 25°C | — | 1.55 | 2.15 | V |
| | | | $I_C$ = 25A, $T_j$ = 125°C | — | 1.65 | 2.25 | |
| $V_{EC}$ | FWD forward voltage | $T_j$ = 25°C, –$I_C$ = 25A, $V_{CIN}$ = 5V | | — | 2.50 | 3.40 | V |
| $t_{on}$ | Switching times | $V_{CC}$ = 300V, $V_D = V_{DB}$ = 15V, $I_C$ = 25A, $T_j$ = 125°C, $V_{CIN}$ = 5V ↔ 0V, Inductive load (upper-lower arm) | | 0.10 | 0.80 | 1.30 | µs |
| $t_{rr}$ | | | | — | 0.10 | — | µs |
| $t_{c(on)}$ | | | | — | 0.30 | 0.70 | µs |
| $t_{off}$ | | | | — | 1.50 | 2.60 | µs |
| $t_{c(off)}$ | | | | — | 0.80 | 1.70 | µs |
| $I_{CES}$ | Collector-emitter cut-off current | $V_{CE} = V_{CES}$ | $T_j$ = 25°C | — | — | 1 | mA |
| | | | $T_j$ = 125°C | — | — | 10 | |

### CONTROL (PROTECTION) PART

| Symbol | Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_D$ | Control supply voltage | Applied between $V_{P1}$-$V_{PC}$, $V_{N1}$-$V_{NC}$ | | 13.5 | 15.0 | 16.5 | V |
| $V_{DB}$ | Control supply voltage | Applied between $V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$, $V_{WFB}$-$V_{WFS}$ | | 13.5 | 15.0 | 16.5 | V |
| $I_D$ | Circuit current | $V_D = V_{DB}$ = 15V, $V_{CIN}$= 5V | Total of $V_{P1}$-$V_{PC}$, $V_{N1}$-$V_{NC}$ | — | — | 8.50 | mA |
| | | | $V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$, $V_{WFB}$-$V_{WFS}$ | — | — | 1.00 | |
| $V_{FOH}$ | Fault output voltage | $V_{SC}$ = 0V, $F_O$ = 10kΩ 5V pull-up | | 4.9 | — | — | V |
| $V_{FOL}$ | | $V_{SC}$ = 1V, $F_O$ = 10kΩ 5V pull-up | | — | 0.8 | 1.2 | V |
| $V_{FOsat}$ | | $V_{SC}$ = 1V, $I_{FO}$ = 15mA | | 0.8 | 1.2 | 1.8 | V |
| $t_{dead}$ | Arm shoot-through blocking time | Relates to corresponding input signal for blocking arm shoot-through. –20°C ≤ $T_C$ ≤ 100°C | | 2.5 | — | — | µs |
| $V_{SC(ref)}$ | Short circuit trip level | $T_j$ = 25°C, $V_D$ = 15V (Note 3) | | 0.45 | 0.5 | 0.55 | V |
| $UV_{DBt}$ | Supply circuit under-voltage protection | $T_j$ ≤ 125°C | Trip level | 10.0 | — | 12.0 | V |
| $UV_{DBr}$ | | | Reset level | 10.5 | — | 12.5 | V |
| $UV_{Dt}$ | | | Trip level | 10.3 | — | 12.5 | V |
| $UV_{Dr}$ | | | Reset level | 10.8 | — | 13.0 | V |
| $t_{FO}$ | Fault output pulse width | $C_{FO}$ = 22nF (Note 4) | | 1.0 | 1.8 | — | ms |
| $V_{th(on)}$ | ON threshold voltage | Applied between : $U_P$, $V_P$, $W_P$-$V_{PC}$, $U_N$, $V_N$, $W_N$-$V_{NC}$ | | 0.8 | 1.4 | 2.0 | V |
| $V_{th(off)}$ | OFF threshold voltage | | | 2.5 | 3.0 | 4.0 | V |

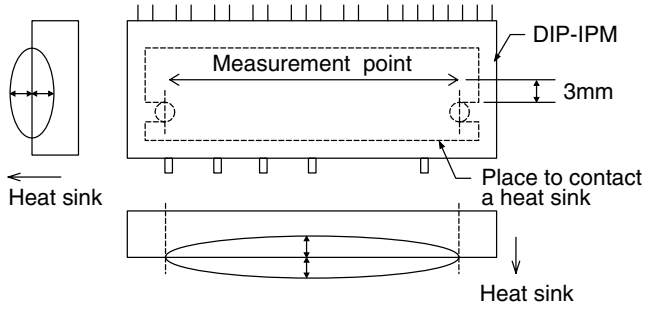
**Note 3 :** Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 42.5 A.

**4 :** Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width $t_{FO}$ depends on the capacitance value of $C_{FO}$ according to the following approximate equation : $C_{FO} = 12.2 \times 10^{-6} \times t_{FO}$ [F].

## MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter | Condition | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Mounting torque | Mounting screw : M4 | — | 0.98 | 1.18 | 1.47 | N·m |
| Terminal pulling strength | Weight 19.6N | EIAJ-ED-4701 | 10 | — | — | s |
| Bending strength | Weight 9.8N. 90deg bend | EIAJ-ED-4701 | 2 | — | — | times |
| Weight | | — | — | 54 | — | g |
| Heat-sink flatness | (Note 5) | — | –50 | — | 100 | μm |

**Note 5: Measurement point of heat-sink flatness**




## RECOMMENDED OPERATION CONDITIONS

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{CC}$ | Supply voltage | Applied between P-N | 0 | 300 | 400 | V |
| $V_D$ | Control supply voltage | Applied between $V_{P1}$-$V_{PC}$, $V_{N1}$-$V_{NC}$ | 13.5 | 15.0 | 16.5 | V |
| $V_{DB}$ | Control supply voltage | Applied between $V_{UFB}$-$V_{UFS}$, $V_{VFB}$-$V_{VFS}$, $V_{WFB}$-$V_{WFS}$ | 13.5 | 15.0 | 16.5 | V |
| $\Delta V_D$, $\Delta V_{DB}$ | Control supply variation | | –1 | — | 1 | V/μs |
| $t_{dead}$ | Arm shoot-through blocking time | Relates to corresponding input signal for blocking arm shoot-through | 2.5 | — | — | μs |
| $f_{PWM}$ | PWM input frequency | $T_C \leq 100°C$, $T_j \leq 125°C$ | — | 5 | — | kHz |
| $V_{CIN(ON)}$ | Input ON threshold voltage | Applied between $U_P$, $V_P$, $W_P$-$V_{PC}$ | 0~0.65 | | | V |
| $V_{CIN(OFF)}$ | Input OFF threshold voltage | Applied between $U_N$, $V_N$, $W_N$-$V_{NC}$ | 4.0~5.5 | | | V |

**Fig. 4 THE DIP-IPM INTERNAL CIRCUIT**

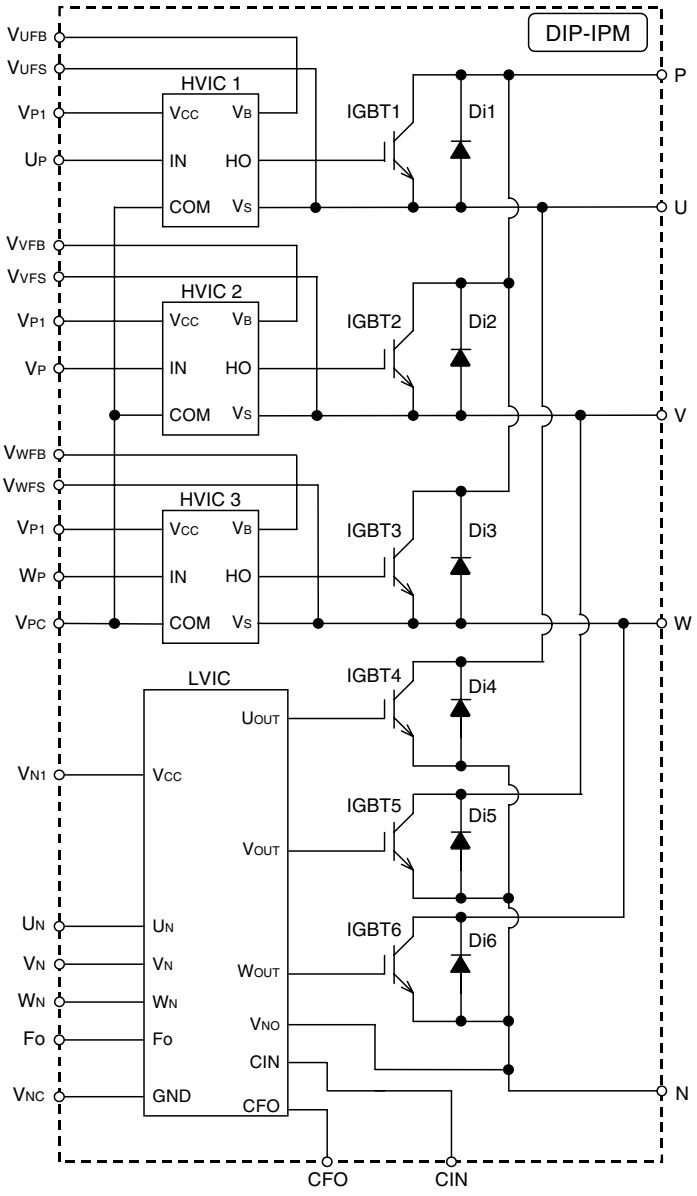
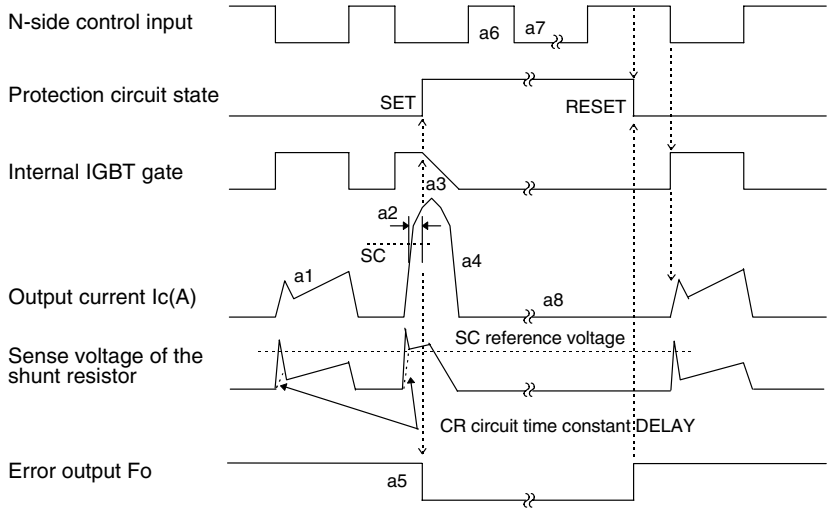


**Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS**

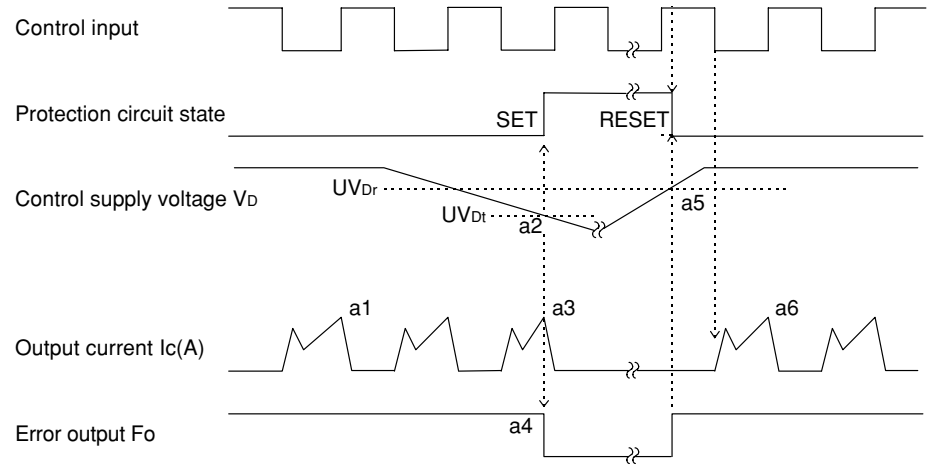
**[A] Short-Circuit Protection (N-side only)**

(For the external shunt resistor and CR connection.)
a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit current detection (SC trigger).
a3. Hard IGBT gate interrupt.
a4. IGBT turns OFF.
a5. FO timer operation starts : The pulse width of the FO signal is set by the external capacitor CFO.
a6. Input "H" : IGBT OFF state.
a7. Input "L" : IGBT ON state.
a8. IGBT OFF state.




**[B] Under-Voltage Protection (N-side, UVD)**

a1. Normal operation : IGBT ON and carrying current.
a2. Under voltage trip (UVDt).
a3. IGBT OFF in spite of control input condition.
a4. FO timer operation starts.
a5. Under voltage reset (UVDr).
a6. Normal operation : IGBT ON and carrying current.



**[C] Under-Voltage Protection (P-side, $UV_{DB}$)**

a1. Control supply voltage rises : After the voltage level reachs $UV_{DBr}$, the circuits start to operate when the next input is applied.
a2. Normal operation : IGBT ON and carrying current.
a3. Under voltage trip ($UV_{DBt}$).
a4. IGBT OFF in spite of control input condition, but there is no $F_O$ signal output.
a5. Under-voltage reset ($UV_{DBr}$).
a6. Normal operation : IGBT ON and carrying current.

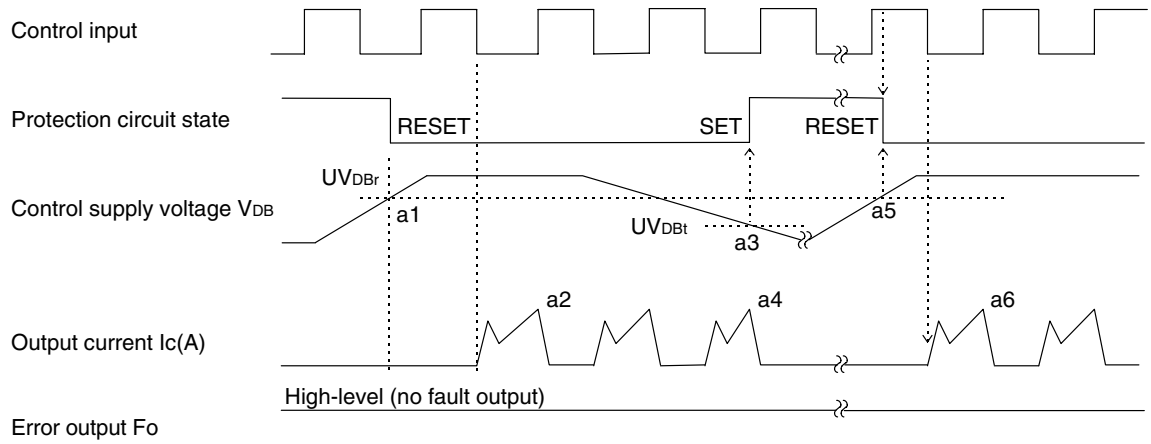
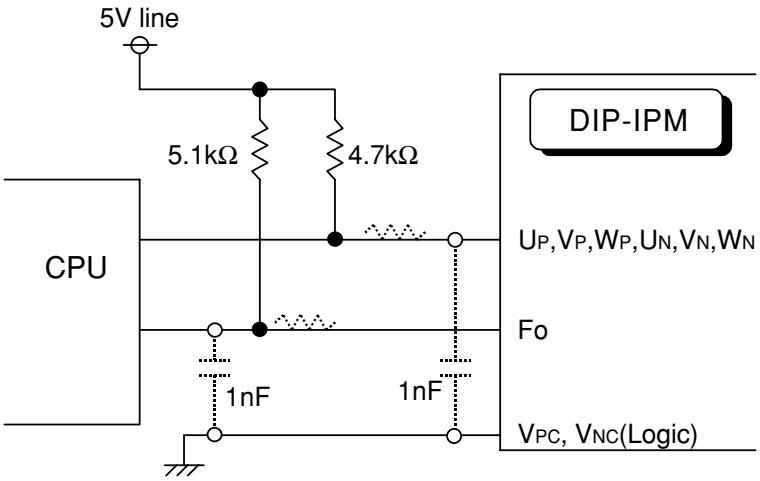
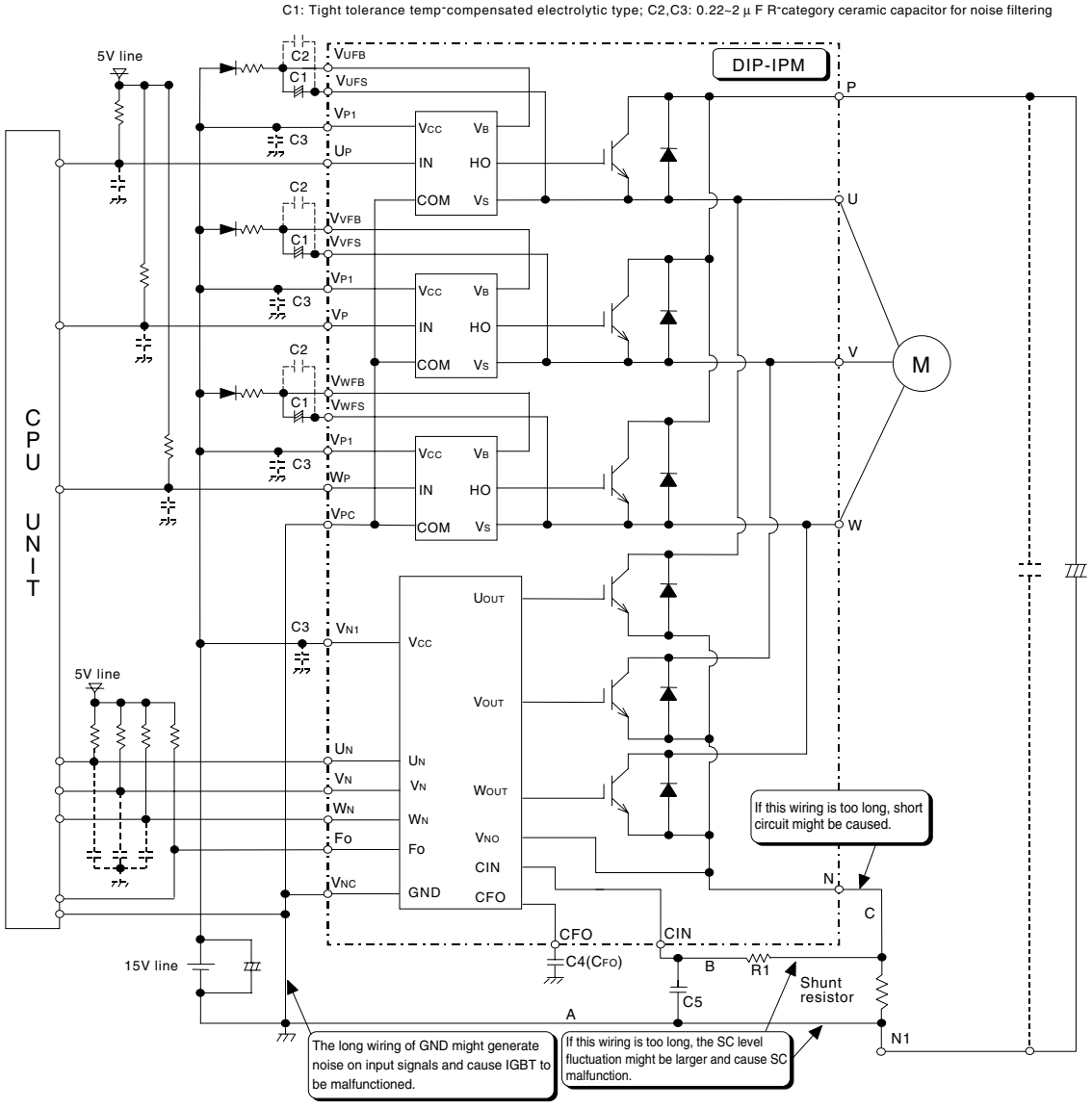



**Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT**




**Note :** RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and on the wiring impedances of the application's printed circuit board.

**Fig. 7 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE**




**Note 1 :** To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible. (Less than 2cm)

**2 :** By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

**3 :** $F_O$ output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1kΩ resistance.

**4 :** $F_O$ output pulse width should be decided by connecting an external capacitor between CFO and $V_{NC}$ terminals ($C_{FO}$). (Example : $C_{FO}$ = 22 nF → $t_{FO}$ = 1.8 ms (typ.))

**5 :** Each input signal line should be pulled up to the 5V power supply with approximately 4.7kΩ resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedances of the system's printed circuit board). Approximately a 0.22~2μF by-pass capacitor should be used across each power supply connection terminals.

**6 :** To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.

**7 :** In the recommended protection circuit, please select the $R_1C_5$ time constant in the range 1.5~2μs.

**8 :** Each capacitor should be put as nearby the pins of the DIP-IPM as possible.

**9 :** To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22μF snubber capacitor between the P&N1 pins is recommended.