

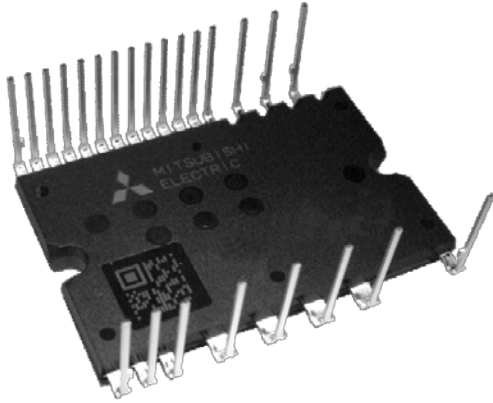
< Dual-In-Line Package Intelligent Power Module >

PSS15S92F6-AG

PSS15S92E6-AG

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 600V / 15A (CSTBT)
- N-side IGBT open emitter
- Built-in bootstrap diodes with current limiting resistor

APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

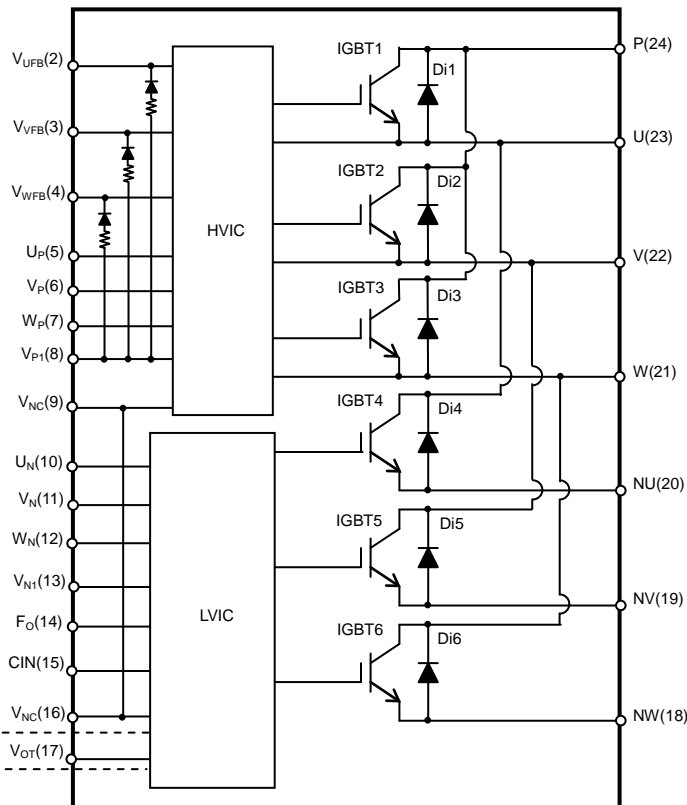
TYPE NAME

| | |
|---------------|----------------------------------|
| PSS15S92F6-AG | With temperature output function |
| PSS15S92E6-AG | With OT protection function |

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC), Over temperature protection (OT, PSS15S92E6-AG only)
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply) and OT fault
- Temperature output : Outputting LVIC temperature by analog signal (PSS15S92F6-AG only)
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



- Built-in temperature output type: V_{OT}
(PSS**S92F6-AG)
- Built-in OT type: NC (No Connection)
(PSS**S92E6-AG)

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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

| Symbol | Parameter | Condition | Ratings | Unit |
|------------------------|------------------------------------|--|----------|------------------|
| V_{CC} | Supply voltage | Applied between P-NU,NV,NW | 450 | V |
| $V_{CC(\text{surge})}$ | Supply voltage (surge) | Applied between P-NU,NV,NW | 500 | V |
| V_{CES} | Collector-emitter voltage | | 600 | V |
| $\pm I_C$ | Each IGBT collector current | $T_C = 25^\circ\text{C}$ (Note 1) | 15 | A |
| $\pm I_{CP}$ | Each IGBT collector current (peak) | $T_C = 25^\circ\text{C}$, less than 1ms | 30 | A |
| P_C | Collector dissipation | $T_C = 25^\circ\text{C}$, per 1 chip | 27.0 | W |
| T_j | Junction temperature | (Note 2) | -30~+150 | $^\circ\text{C}$ |

Note1: Pulse width and period are limited due to junction temperature.

Note2: The maximum junction temperature rating of built-in power chips is 150°C ($@T_C \leq 100^\circ\text{C}$). However, to ensure safe operation of DIPIPM, the average junction temperature should be limited to $T_{j(\text{Ave})} \leq 125^\circ\text{C}$ ($@T_C \leq 100^\circ\text{C}$).

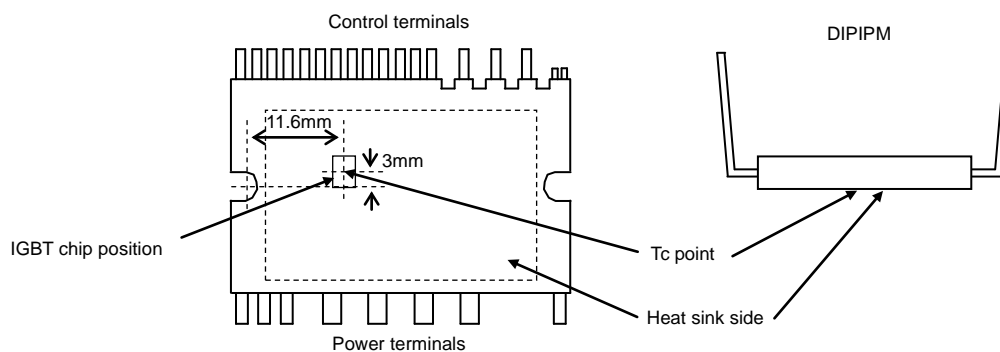
CONTROL (PROTECTION) PART

| Symbol | Parameter | Condition | Ratings | Unit |
|----------|-------------------------------|--|-----------------|------|
| V_D | Control supply voltage | Applied between $V_{P1}-V_{NC}, V_{N1}-V_{NC}$ | 20 | V |
| V_{DB} | Control supply voltage | Applied between $V_{UFB}-U, V_{VFB}-V, V_{WFB}-W$ | 20 | V |
| V_{IN} | Input voltage | Applied between $U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}$ | -0.5~ $V_D+0.5$ | V |
| V_{FO} | Fault output supply voltage | Applied between F_O-V_{NC} | -0.5~ $V_D+0.5$ | V |
| I_{FO} | Fault output current | Sink current at F_O terminal | 1 | mA |
| V_{SC} | Current sensing input voltage | Applied between $CIN-V_{NC}$ | -0.5~ $V_D+0.5$ | V |

TOTAL SYSTEM

| Symbol | Parameter | Condition | Ratings | Unit |
|-----------------------|--|---|----------|------------------|
| $V_{CC(\text{PROT})}$ | Self protection supply voltage limit (Short circuit protection capability) | $V_D = 13.5\sim 16.5\text{V}$, Inverter Part $T_j = 125^\circ\text{C}$, non-repetitive, less than $2\mu\text{s}$ | 400 | V |
| T_C | Module case operation temperature | Measurement point of T_C is provided in Fig.1 | -30~+100 | $^\circ\text{C}$ |
| T_{sig} | Storage temperature | | -40~+125 | $^\circ\text{C}$ |
| V_{iso} | Isolation voltage | 60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate | 1500 | V_{rms} |

Fig. 1: T_C MEASUREMENT POINT



THERMAL RESISTANCE

| Symbol | Parameter | Condition | Limits | | | Unit |
|-----------------------|--|-------------------------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| $R_{\text{th}(j-c)Q}$ | Junction to case thermal resistance (Note 3) | Inverter IGBT part (per 1/6 module) | - | - | 3.7 | K/W |
| $R_{\text{th}(j-c)F}$ | | Inverter FWDi part (per 1/6 module) | - | - | 4.5 | K/W |

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about $+100\mu\text{m}\sim +200\mu\text{m}$ on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink $R_{\text{th}(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{\text{th}(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: $20\mu\text{m}$, thermal conductivity: $1.0\text{W/m}\cdot\text{k}$).

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ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

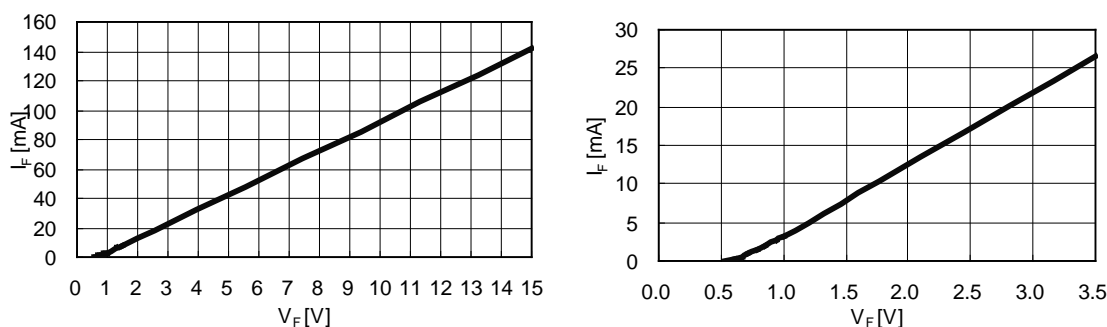
| Symbol | Parameter | Condition | Limits | | | Unit | |
|---------------|--------------------------------------|---|------------------------------------|------|------|---------------|----|
| | | | Min. | Typ. | Max. | | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_D=V_{DB} = 15V, V_{IN}= 5V$ | $I_C= 15A, T_j= 25^\circ\text{C}$ | - | 1.70 | 2.05 | V |
| | | | $I_C= 15A, T_j= 125^\circ\text{C}$ | - | 1.90 | 2.25 | |
| | | | $I_C=1.5A, T_j= 25^\circ\text{C}$ | - | 0.90 | 1.10 | |
| V_{EC} | FWDi forward voltage | $V_{IN}= 0V, -I_C= 15A$ | - | 2.50 | 3.00 | V | |
| t_{on} | Switching times | $V_{CC}= 300V, V_D= V_{DB}= 15V$ $I_C= 15A, T_j= 125^\circ\text{C}, V_{IN}= 0\leftrightarrow 5V$ Inductive Load (upper-lower arm) | 0.65 | 1.05 | 1.45 | μs | |
| $t_{C(on)}$ | | | - | 0.40 | 0.65 | μs | |
| t_{off} | | | - | 1.15 | 1.60 | μs | |
| $t_{C(off)}$ | | | - | 0.15 | 0.30 | μs | |
| t_{rr} | | | - | 0.30 | - | μs | |
| I_{CES} | Collector-emitter cut-off current | $V_{CE}=V_{CES}$ | $T_j= 25^\circ\text{C}$ | - | - | 1 | mA |
| | | | $T_j= 125^\circ\text{C}$ | - | - | 10 | |

CONTROL (PROTECTION) PART

| Symbol | Parameter | Condition | Limits | | | Unit | |
|---------------|---|--|--------------------------------------|-------|-------|---------------|------------------|
| | | | Min. | Typ. | Max. | | |
| I_D | Circuit current | Total of $V_{P1}-V_{NC}, V_{N1}-V_{NC}$ | $V_D=15V, V_{IN}=0V$ | - | - | 2.80 | mA |
| | | | $V_D=15V, V_{IN}=5V$ | - | - | 2.80 | |
| I_{DB} | | Each part of $V_{UFB}-U, V_{VFB}-V, V_{WFB}-W$ | $V_D=V_{DB}=15V, V_{IN}=0V$ | - | - | 0.10 | |
| | | | $V_D=V_{DB}=15V, V_{IN}=5V$ | - | - | 0.10 | |
| $V_{SC(ref)}$ | Short circuit trip level | $V_D = 15V$ (Note 4) | 0.455 | 0.480 | 0.505 | V | |
| UV_{DBt} | P-side Control supply under-voltage protection(UV) | $T_j \leq 125^\circ\text{C}$ | Trip level | 7.0 | 10.0 | 12.0 | V |
| UV_{DBr} | | | Reset level | 7.0 | 10.0 | 12.0 | V |
| UV_{Dt} | N-side Control supply under-voltage protection(UV) | $T_j \leq 125^\circ\text{C}$ | Trip level | 10.3 | - | 12.5 | V |
| UV_{Dr} | | | Reset level | 10.8 | - | 13.0 | V |
| V_{OT} | Temperature Output (PSS**S92E6-AG) | Pull down $R=5k\Omega$ (Note 5) | LVIC Temperature= 90°C | 2.63 | 2.77 | 2.91 | V |
| | | | LVIC Temperature= 25°C | 0.88 | 1.13 | 1.39 | V |
| OT_t | Over temperature protection (OT, PSS**S92E6-AG) (Note6) | $V_D = 15V$ Detect LVIC temperature | Trip level | 100 | 120 | 140 | $^\circ\text{C}$ |
| OT_{th} | | | Hysteresis of trip-reset | - | 10 | - | $^\circ\text{C}$ |
| V_{FOH} | Fault output voltage | $V_{SC} = 0V, F_O$ terminal pulled up to 5V by 10k Ω $V_{SC} = 1V, I_{FO} = 1mA$ | 4.9 | - | - | V | |
| V_{FOL} | | | - | - | 0.95 | V | |
| t_{FO} | Fault output pulse width | (Note 7) | 20 | - | - | μs | |
| I_{IN} | Input current | $V_{IN} = 5V$ | 0.70 | 1.00 | 1.50 | mA | |
| $V_{th(on)}$ | ON threshold voltage | Applied between $U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}$ | - | 2.10 | 2.60 | V | |
| $V_{th(off)}$ | OFF threshold voltage | | 0.80 | 1.30 | - | | |
| $V_{th(hys)}$ | ON/OFF threshold hysteresis voltage | | 0.35 | 0.65 | - | | |
| V_F | Bootstrap Di forward voltage | $I_F=10mA$ including voltage drop by limiting resistor (Note 8) | 1.1 | 1.7 | 2.3 | V | |
| R | Built-in limiting resistance | Included in bootstrap Di | 80 | 100 | 120 | Ω | |

- Note 4 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.
 5 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. Temperature of LVIC vs. VOT output characteristics is described in Fig. 3.
 6 : When the LVIC temperature exceeds OT trip temperature level(OT_t), OT protection works and Fo outputs. In that case if the heat sink dropped off or fixed loosely, don't reuse that DIPIPM. (There is a possibility that junction temperature of power chips exceeded maximum $T_j(150^\circ\text{C})$).
 7 : Fault signal Fo outputs when SC, UV or OT protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 20 μs), but at UV or OT failure, Fo outputs continuously until recovering from UV or OT state. (But minimum Fo pulse width is 20 μs).
 8 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of bootstrap Di V_F-I_F curve (@ $T_a=25^\circ\text{C}$) including voltage drop by limiting resistor (Right chart is enlarged chart.)



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Fig. 3 Temperature of LVIC vs. V_{OT} output characteristics

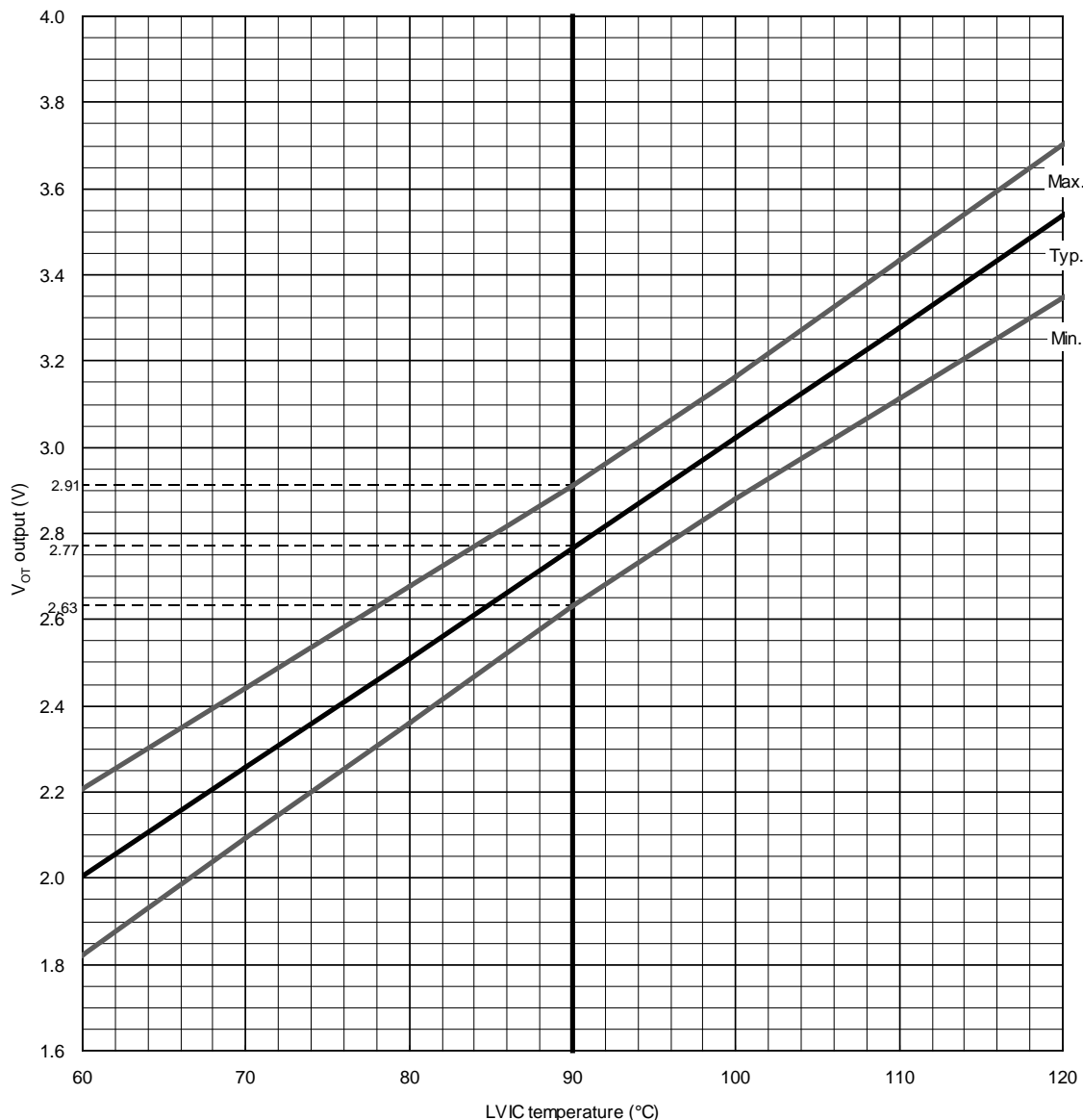
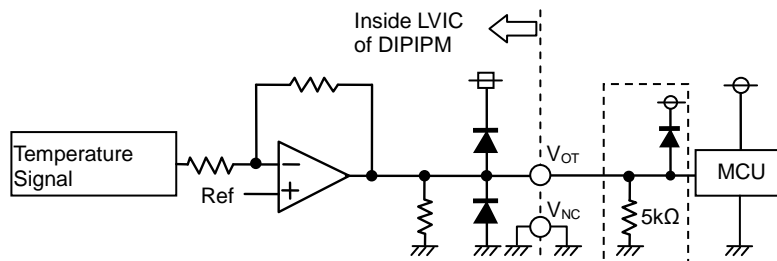


Fig. 4 V_{OT} output circuit



- (1) It is recommended to insert 5k Ω (5.1k Ω is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
- (2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.
- (3) In the case of not using V_{OT} , leave V_{OT} output NC (No Connection).

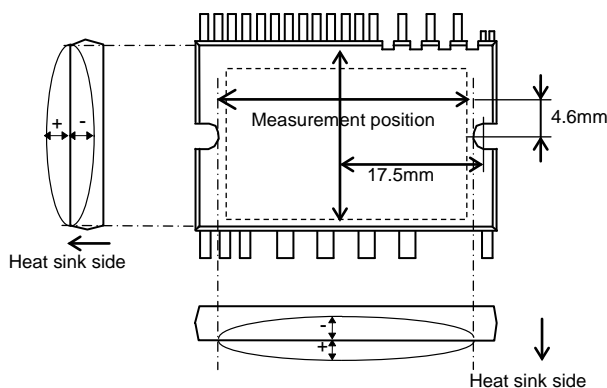
Refer the application note for Super Mini DIPIM Ver.5 series about the usage of V_{OT} .

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MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter | Condition | | Limits | | | Unit |
|---------------------------|--|---------------------|--------|------|------|-------|
| | | | Min. | Typ. | Max. | |
| Mounting torque | Mounting screw : M3 (Note 9) | Recommended 0.69N·m | 0.59 | 0.69 | 0.78 | N·m |
| Terminal pulling strength | Control terminal: Load 4.9N Power terminal: Load 9.8N | EIAJ-ED-4701 | 10 | - | - | s |
| Terminal bending strength | Control terminal: Load 2.45N Power terminal: Load 4.9N 90deg. bend | EIAJ-ED-4701 | 2 | - | - | times |
| Weight | | | - | 8.5 | - | g |
| Heat-sink flatness | (Note 10) | | -50 | - | 100 | μm |

Note 9: Plain washers (ISO 7089-7094) are recommended.
 Note 10: Measurement point of heat sink flatness



RECOMMENDED OPERATION CONDITIONS

| Symbol | Parameter | Condition | Limits | | | Unit | |
|-----------------------------|---------------------------------|--|--------------------------|------|------|------|------|
| | | | Min. | Typ. | Max. | | |
| V_{CC} | Supply voltage | Applied between P-NU, NV, NW | 0 | 300 | 400 | V | |
| V_D | Control supply voltage | Applied between $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$ | 13.5 | 15.0 | 16.5 | V | |
| V_{DB} | Control supply voltage | Applied between $V_{UFB}-U$, $V_{VFB}-V$, $V_{WFB}-W$ | 13.0 | 15.0 | 18.5 | V | |
| $\Delta V_D, \Delta V_{DB}$ | Control supply variation | | -1 | - | +1 | V/μs | |
| t_{dead} | Arm shoot-through blocking time | For each input signal | 1.0 | - | - | μs | |
| f_{PWM} | PWM input frequency | $T_C \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$ | - | - | 20 | kHz | |
| I_O | Allowable r.m.s. current | $V_{CC} = 300\text{V}$, $V_D = 15\text{V}$, P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ\text{C}$, $T_j \leq 125^\circ\text{C}$ (Note11) | $f_{PWM} = 5\text{kHz}$ | - | - | 7.5 | Arms |
| | | | $f_{PWM} = 15\text{kHz}$ | - | - | 4.5 | |
| $PW_{IN}(on)$ | Minimum input pulse width | (Note 12) | 0.7 | - | - | μs | |
| $PW_{IN}(off)$ | | | 0.7 | - | - | | |
| V_{NC} | V_{NC} variation | Between $V_{NC}-NU$, NV, NW (including surge) | -5.0 | - | +5.0 | V | |
| T_j | Junction temperature | | -20 | - | +125 | °C | |

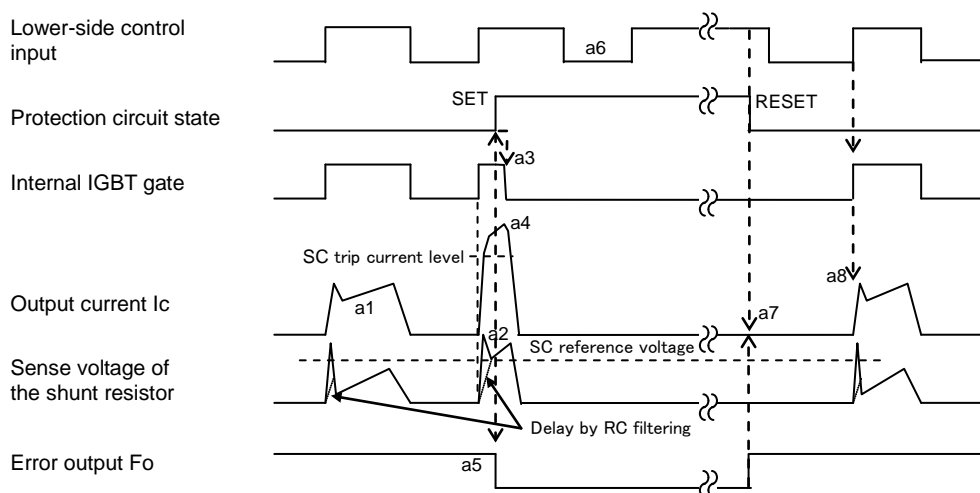
Note 11: Allowable r.m.s. current depends on the actual application conditions.
 Note 12: DIPIPM might not make response if the input signal pulse width is less than $PW_{IN}(on)$, $PW_{IN}(off)$.

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Fig. 5 Timing Charts of The DIPIPM Protective Functions

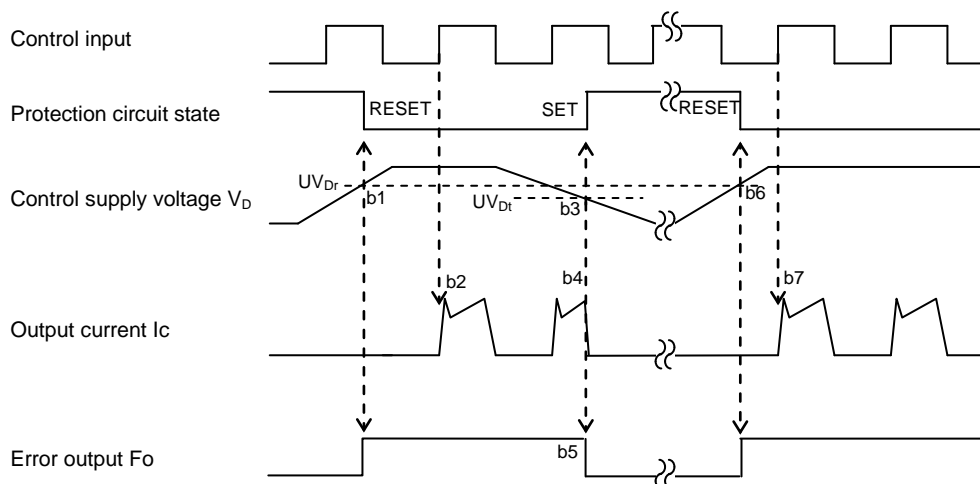
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger)
 (It is recommended to set RC time constant 1.5~2.0 μ s so that IGBT shut down within 2.0 μ s when SC.)
- a3. All N-side IGBT's gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. F_O outputs for t_{Fo}=minimum 20 μ s.
- a6. Input = "L": IGBT OFF
- a7. F_o finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
 (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.



[B] Under-Voltage Protection (N-side, UV_D)

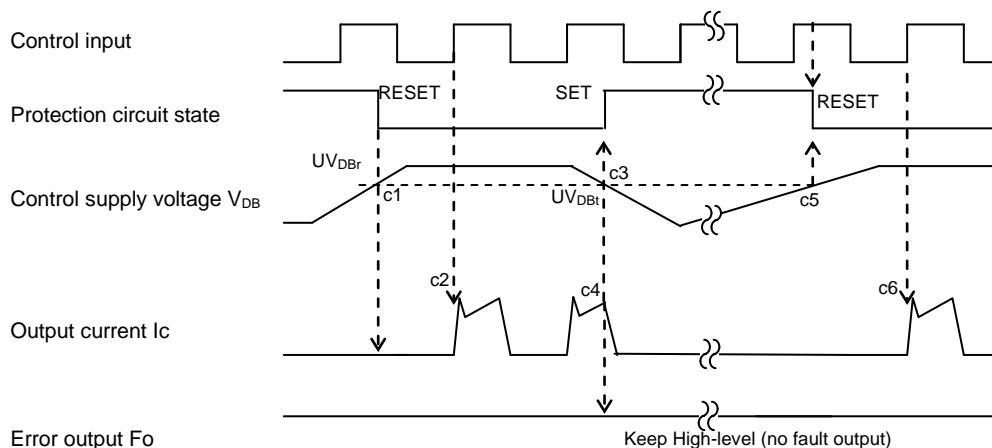
- b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L→H).
 (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: IGBT ON and outputs current.
- b3. V_D level drops to under voltage trip level. (UV_{Dt}).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5. F_o outputs for t_{Fo}=minimum 20 μ s, but output is extended during V_D keeps below UV_{Dr}.
- b6. V_D level reaches UV_{Dr}.
- b7. Normal operation: IGBT ON and outputs current.



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[C] Under-Voltage Protection (P-side, UV_{DB})

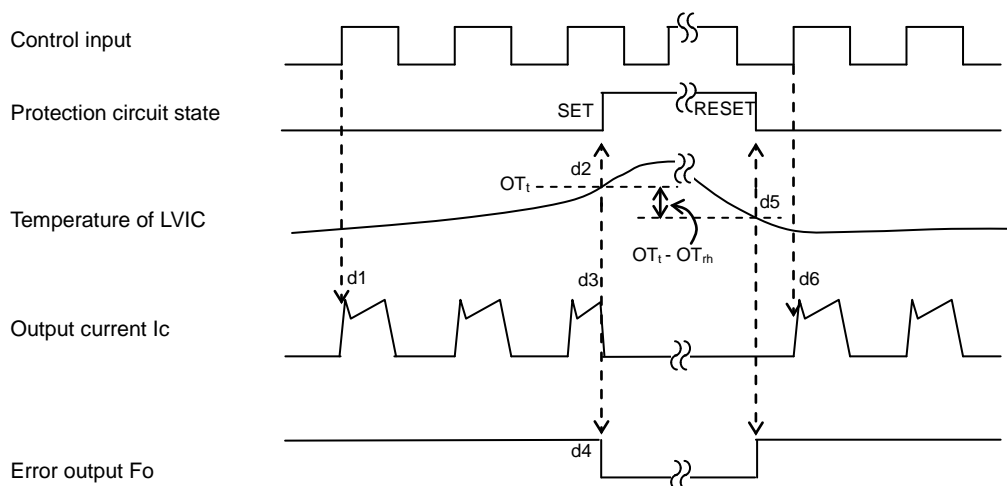
- c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr} , IGBT turns on by next ON signal (L→H).
- c2. Normal operation: IGBT ON and outputs current.
- c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
- c4. IGBT of the correspond phase only turns OFF in spite of control input signal level, but there is no F_o signal output.
- c5. V_{DB} level reaches UV_{DBr} .
- c6. Normal operation: IGBT ON and outputs current.



[D] Over Temperature Protection (N-side, Detecting LVIC temperature)

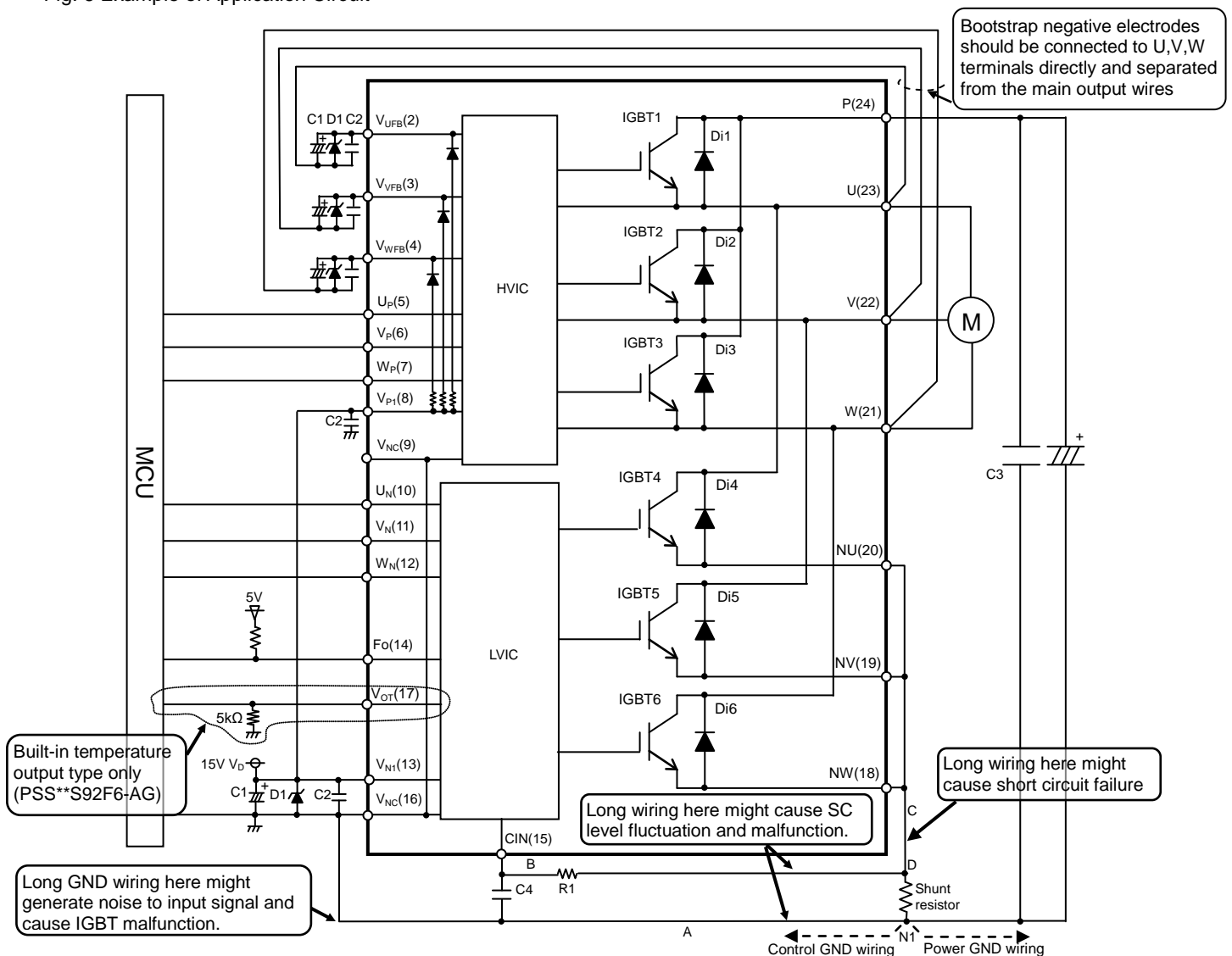
- d1. Normal operation: IGBT ON and outputs current.
- d2. LVIC temperature exceeds over temperature trip level (OT_t).
- d3. All N-side IGBTs turn OFF in spite of control input condition.
- d4. F_o outputs for t_{Fo} =minimum 20 μ s, but output is extended during LVIC temperature keeps over OT_t .
- d5. LVIC temperature drops to over temperature reset level.
- d6. Normal operation: IGBT turns on by next ON signal (L→H).

(IGBT of each phase can return to normal state by inputting ON signal to each phase.)



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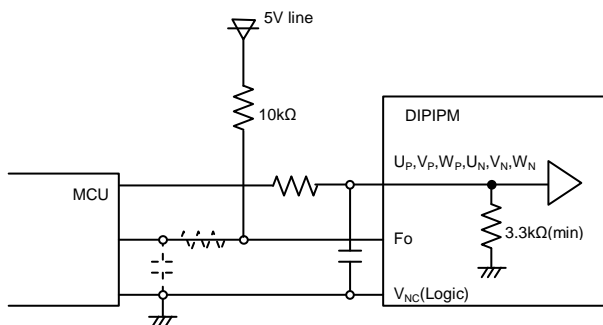
Fig. 6 Example of Application Circuit



- (1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
- (2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
- (3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22 μ F snubber capacitor C3 between the P-N1 terminals is recommended.
- (4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2 μ s. (1.5 μ s~2 μ s is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
- (5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
- (6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.
- (7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.22 μ -2 μ F, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- (8) Input drive is High-active type. There is a minimum 3.3k Ω pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
- (9) F_o output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (I_{Fo} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10k Ω (5k Ω or more) is recommended.)
- (10) Thanks to built-in HVIC, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
- (11) Two V_{NC} terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.
- (12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt \leq +/-1V/ μ s, Vrippl \leq 2Vp-p.
- (13) For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.

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Fig. 7 MCU I/O Interface Circuit

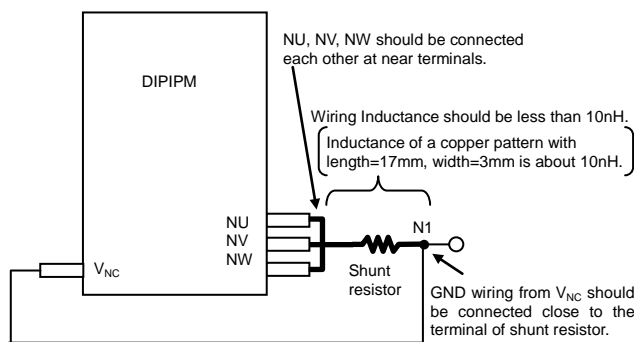


Note)

Design for input RC filter depends on PWM control scheme used in the application and wiring impedance of the printed circuit board. DIPIPM input signal interface integrates a minimum 3.3kΩ pull-down resistor. Therefore, when inserting RC filter, it is necessary to satisfy turn-on threshold voltage requirement.

F_o output is open drain type. It should be pulled up to control power supply (e.g. 5V, 15V) with a resistor that makes F_o sink current I_{Fo} 1mA or less. In the case of pulled up to 5V supply, 10kΩ (5kΩ or more) is recommended.

Fig. 8 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

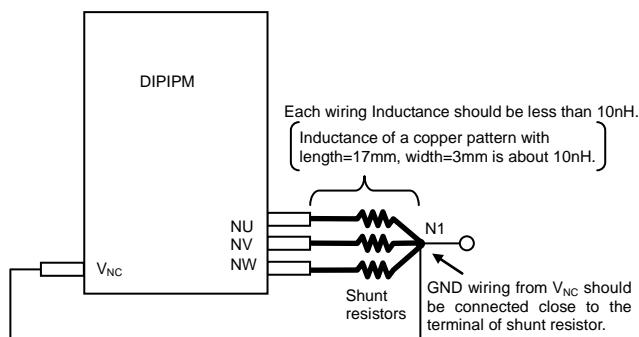
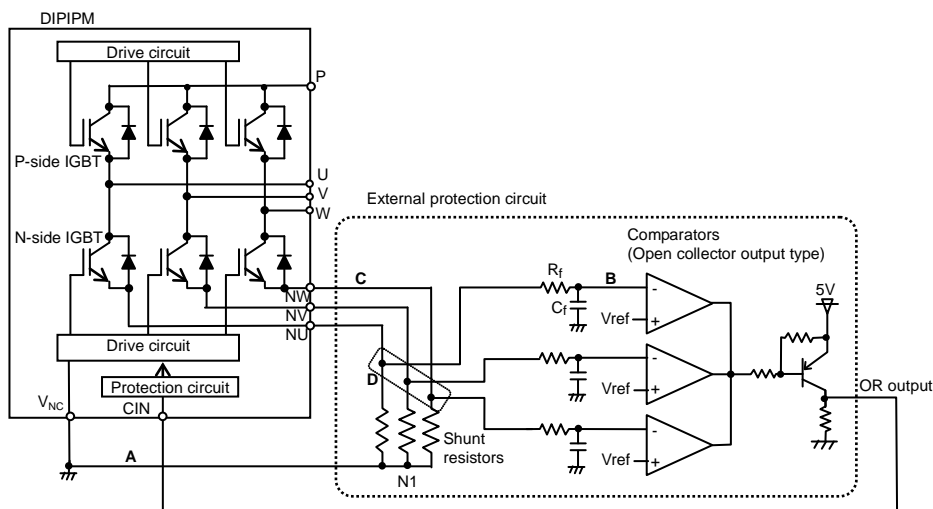


Fig. 9 Pattern Wiring Around the Shunt Resistor (for the case of open emitter)

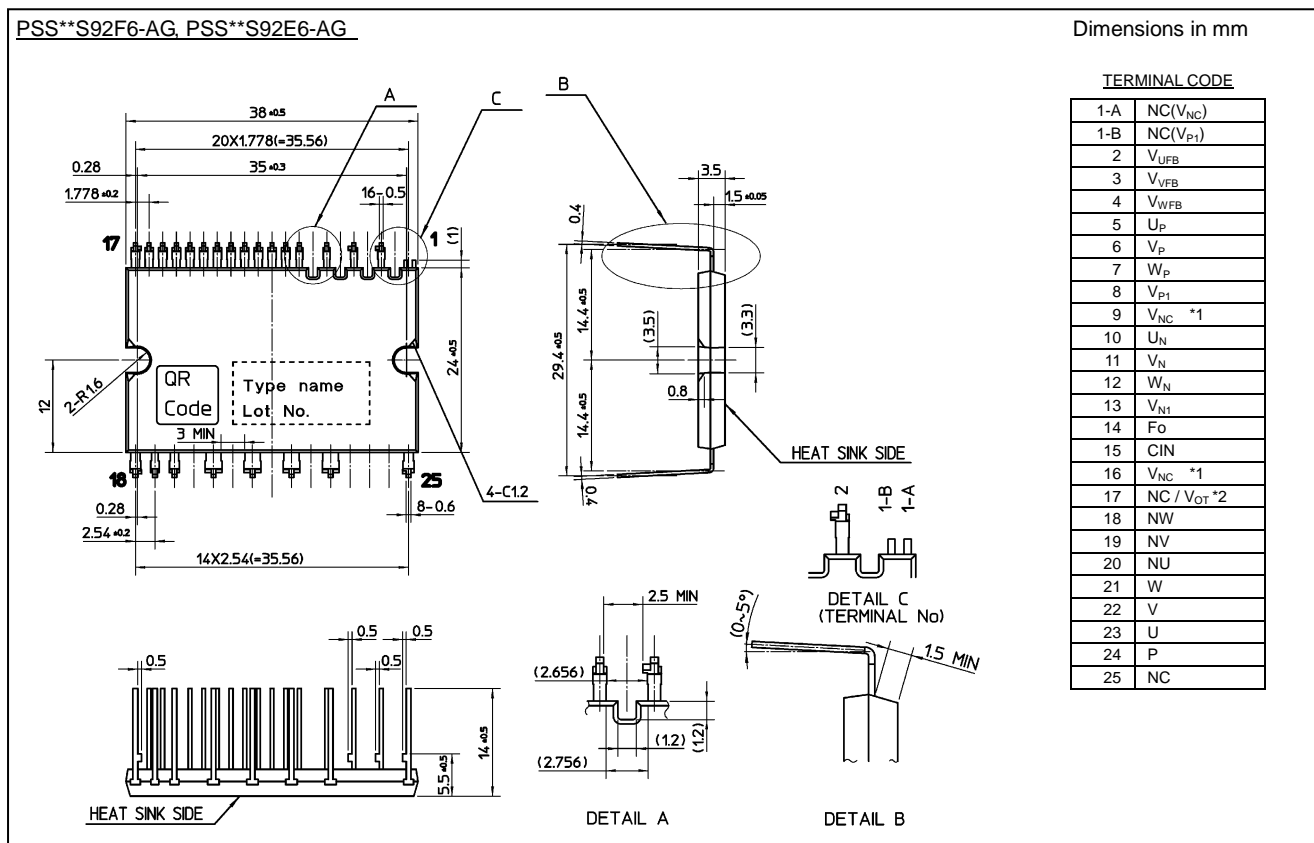
When DIPIPM is operated with three shunt resistors, voltage of each shunt resistor cannot be input to CIN terminal directly. In that case, it is necessary to use the external protection circuit as below.



- (1) It is necessary to set the time constant $R_f C_f$ of external comparator input so that IGBT stops within $2\mu s$ when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) It is recommended for the threshold voltage V_{ref} to set to the same rating of short circuit trip level ($V_{sc(ref)}$: typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified value (=1.7 times of rating current).
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be close to the terminal of shunt resistor.
- (6) OR output high level when protection works should be over 0.505V (=maximum $V_{sc(ref)}$ rating).

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 INSULATED TYPE

Fig. 10 Package Outlines



- 1) 9 & 16 pins (V_{NC}) are connected inside DIPIPM, please connect either one to the control power supply GND outside and leave another one open.
- 2) No.17 is V_{OT} for built-in temperature output function type (PSS**S92F6-AG) and NC (No Connection) for built-in OT protection function type (PSS**S92E6-AG).

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Revision Record

| Rev. | Date | Page | Revised contents |
|------|------------|------|------------------|
| 1 | 15/10/2013 | - | New |
| 2 | 15/ 3/2014 | 2 | Add Note 1 |

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