

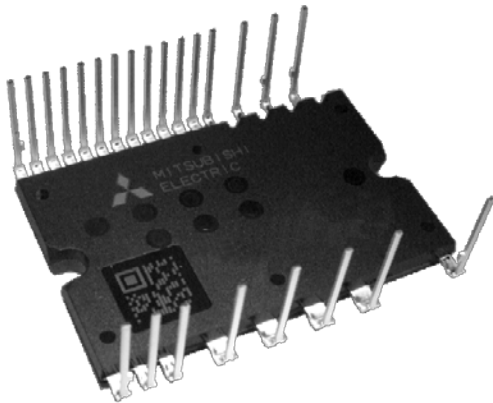
< Dual-In-Line Package Intelligent Power Module >

PSS30S92F6-AG

PSS30S92E6-AG

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 600V / 30A (CSTBT)
- N-side IGBT open emitter
- Built-in bootstrap diodes with current limiting resistor

APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

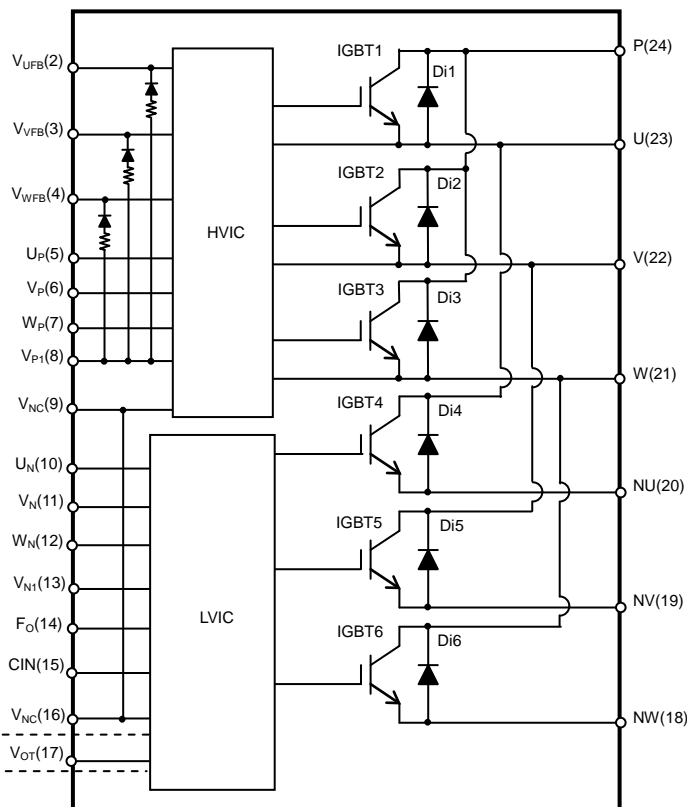
TYPE NAME

PSS30S92F6-AG	With temperature output function
PSS30S92E6-AG	With OT protection function

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC), Over temperature protection (OT, PSS30S92E6-AG only)
- Fault signaling : Corresponding to SC fault (N-side IGBT), UV fault (N-side supply) and OT fault
- Temperature output : Outputting LVIC temperature by analog signal (PSS30S92F6-AG only)
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



- Built-in temperature output type: V_{OT}
(PSS**S92F6-AG)
- Built-in OT type: NC (No Connection)
(PSS**S92E6-AG)

< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
 TRANSFER MOLDING TYPE
 INSULATED TYPE

MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-NU,NV,NW	450	V
$V_{CC(\text{surge})}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
V_{CES}	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$ (Note 1)	30	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$, less than 1ms	60	A
P_C	Collector dissipation	$T_C = 25^\circ\text{C}$, per 1 chip	47.6	W
T_j	Junction temperature	(Note 2)	-30~+150	$^\circ\text{C}$

Note1: Pulse width and period are limited due to junction temperature.

Note2: The maximum junction temperature rating of built-in power chips is 150°C ($@T_C \leq 100^\circ\text{C}$). However, to ensure safe operation of DIPIPM, the average junction temperature should be limited to $T_{j(\text{Ave})} \leq 125^\circ\text{C}$ ($@T_C \leq 100^\circ\text{C}$).

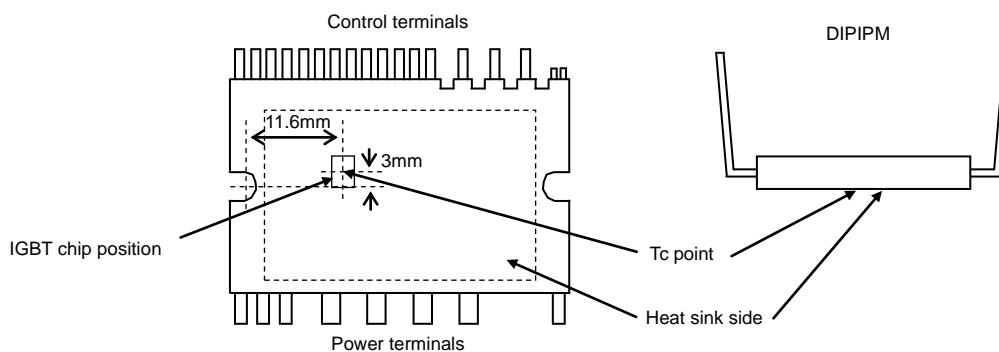
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between $V_{P1}-V_{NC}, V_{N1}-V_{NC}$	20	V
V_{DB}	Control supply voltage	Applied between $V_{UFB}-U, V_{VFB}-V, V_{WFB}-W$	20	V
V_{IN}	Input voltage	Applied between $U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}$	-0.5~ $V_D+0.5$	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~ $V_D+0.5$	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5~ $V_D+0.5$	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(\text{PROT})}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$, Inverter Part $T_j = 125^\circ\text{C}$, non-repetitive, less than $2\mu\text{s}$	400	V
T_C	Module case operation temperature	Measurement point of T_C is provided in Fig.1	-30~+100	$^\circ\text{C}$
T_{sig}	Storage temperature		-40~+125	$^\circ\text{C}$
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}

Fig. 1: T_C MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	-	-	2.1	K/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	-	-	3.0	K/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about $+100\mu\text{m}\sim +200\mu\text{m}$ on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink $R_{th(c-f)}$ is determined by the thickness and the thermal conductivity of the applied grease. For reference, $R_{th(c-f)}$ is about 0.3K/W (per 1/6 module, grease thickness: $20\mu\text{m}$, thermal conductivity: $1.0\text{W/m}\cdot\text{k}$).

< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
 TRANSFER MOLDING TYPE
 INSULATED TYPE

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

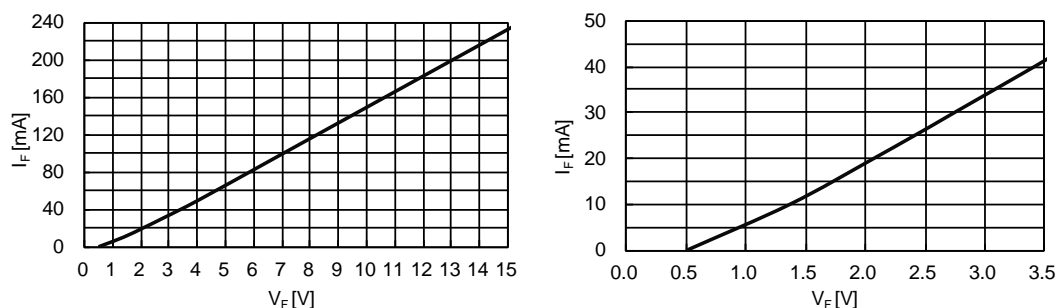
Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D=V_{DB} = 15\text{V}, V_{IN}= 5\text{V}$	$I_C= 30\text{A}, T_j= 25^\circ\text{C}$	-	1.65	2.00	V
			$I_C= 30\text{A}, T_j= 125^\circ\text{C}$	-	1.85	2.20	
			$I_C=3.0\text{A}, T_j= 25^\circ\text{C}$	-	0.90	1.10	
V_{EC}	FWDi forward voltage	$V_{IN}= 0\text{V}, -I_C= 30\text{A}$	-	2.30	2.80	V	
t_{on}	Switching times	$V_{CC}= 300\text{V}, V_D= V_{DB}= 15\text{V}$ $I_C= 30\text{A}, T_j= 125^\circ\text{C}, V_{IN}= 0\leftrightarrow 5\text{V}$ Inductive Load (upper-lower arm)	0.90	1.55	2.30	μs	
$t_{C(on)}$			-	0.40	0.65	μs	
t_{off}			-	1.65	2.40	μs	
$t_{C(off)}$			-	0.15	0.30	μs	
t_{rr}			-	0.30	-	μs	
I_{CES}	Collector-emitter cut-off current	$V_{CE}=V_{CES}$	$T_j= 25^\circ\text{C}$	-	-	1	mA
			$T_j= 125^\circ\text{C}$	-	-	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I_D	Circuit current	Total of $V_{P1}-V_{NC}, V_{N1}-V_{NC}$	$V_D=15\text{V}, V_{IN}=0\text{V}$	-	-	3.40	mA
			$V_D=15\text{V}, V_{IN}=5\text{V}$	-	-	3.40	
I_{DB}		Each part of $V_{UFB}-U,$ $V_{VFB}-V, V_{WFB}-W$	$V_D=V_{DB}=15\text{V}, V_{IN}=0\text{V}$	-	-	0.30	mA
			$V_D=V_{DB}=15\text{V}, V_{IN}=5\text{V}$	-	-	0.30	
$V_{SC(ref)}$	Short circuit trip level	$V_D = 15\text{V}$ (Note 4)	0.455	0.480	0.505	V	
UV_{DBt}	P-side Control supply under-voltage protection(UV)	$T_j \leq 125^\circ\text{C}$	Trip level	10.0	-	12.0	V
UV_{DBr}			Reset level	10.5	-	12.5	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)	$T_j \leq 125^\circ\text{C}$	Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
V_{OT}	Temperature Output (PSS**S92E6-AG) (Note 5)	Pull down $R=5\text{k}\Omega$	LVIC Temperature= 90°C	2.63	2.77	2.91	V
			LVIC Temperature= 25°C	0.88	1.13	1.39	V
OT_t	Over temperature protection (OT, PSS**S92E6-AG) (Note6)	$V_D = 15\text{V}$ Detect LVIC temperature	Trip level	100	120	140	$^\circ\text{C}$
OT_{th}			Hysteresis of trip-reset	-	10	-	$^\circ\text{C}$
V_{FOH}	Fault output voltage	$V_{SC} = 0\text{V}, F_O$ terminal pulled up to 5V by 10k Ω $V_{SC} = 1\text{V}, I_{FO} = 1\text{mA}$	4.9	-	-	V	
V_{FOL}			-	-	0.95	V	
t_{FO}	Fault output pulse width	(Note 7)	20	-	-	μs	
I_{IN}	Input current	$V_{IN} = 5\text{V}$	0.70	1.00	1.50	mA	
$V_{th(on)}$	ON threshold voltage	Applied between $U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}$	-	2.10	2.60	V	
$V_{th(off)}$	OFF threshold voltage		0.80	1.30	-		
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage		0.35	0.65	-		
V_F	Bootstrap Di forward voltage	$I_F=10\text{mA}$ including voltage drop by limiting resistor (Note 8)	0.9	1.3	1.7	V	
R	Built-in limiting resistance	Included in bootstrap Di	48	60	72	Ω	

Note 4 : SC protection works only for N-side IGBT. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.
 5 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. Temperature of LVIC vs. VOT output characteristics is described in Fig. 3.
 6 : When the LVIC temperature exceeds OT trip temperature level(OT_t), OT protection works and F_O outputs. In that case if the heat sink dropped off or fixed loosely, don't reuse that DIPIPM. (There is a possibility that junction temperature of power chips exceeded maximum $T_j(150^\circ\text{C})$).
 7 : Fault signal F_O outputs when SC, UV or OT protection works. F_O pulse width is different for each protection modes. At SC failure, F_O pulse width is a fixed width (=minimum 20 μs), but at UV or OT failure, F_O outputs continuously until recovering from UV or OT state. (But minimum F_O pulse width is 20 μs).
 8 : The characteristics of bootstrap Di is described in Fig.2.

Fig. 2 Characteristics of bootstrap Di V_F - I_F curve (@ $T_a=25^\circ\text{C}$) including voltage drop by limiting resistor (Right chart is enlarged chart.)



< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
 TRANSFER MOLDING TYPE
 INSULATED TYPE

Fig. 3 Temperature of LVIC vs. V_{OT} output characteristics

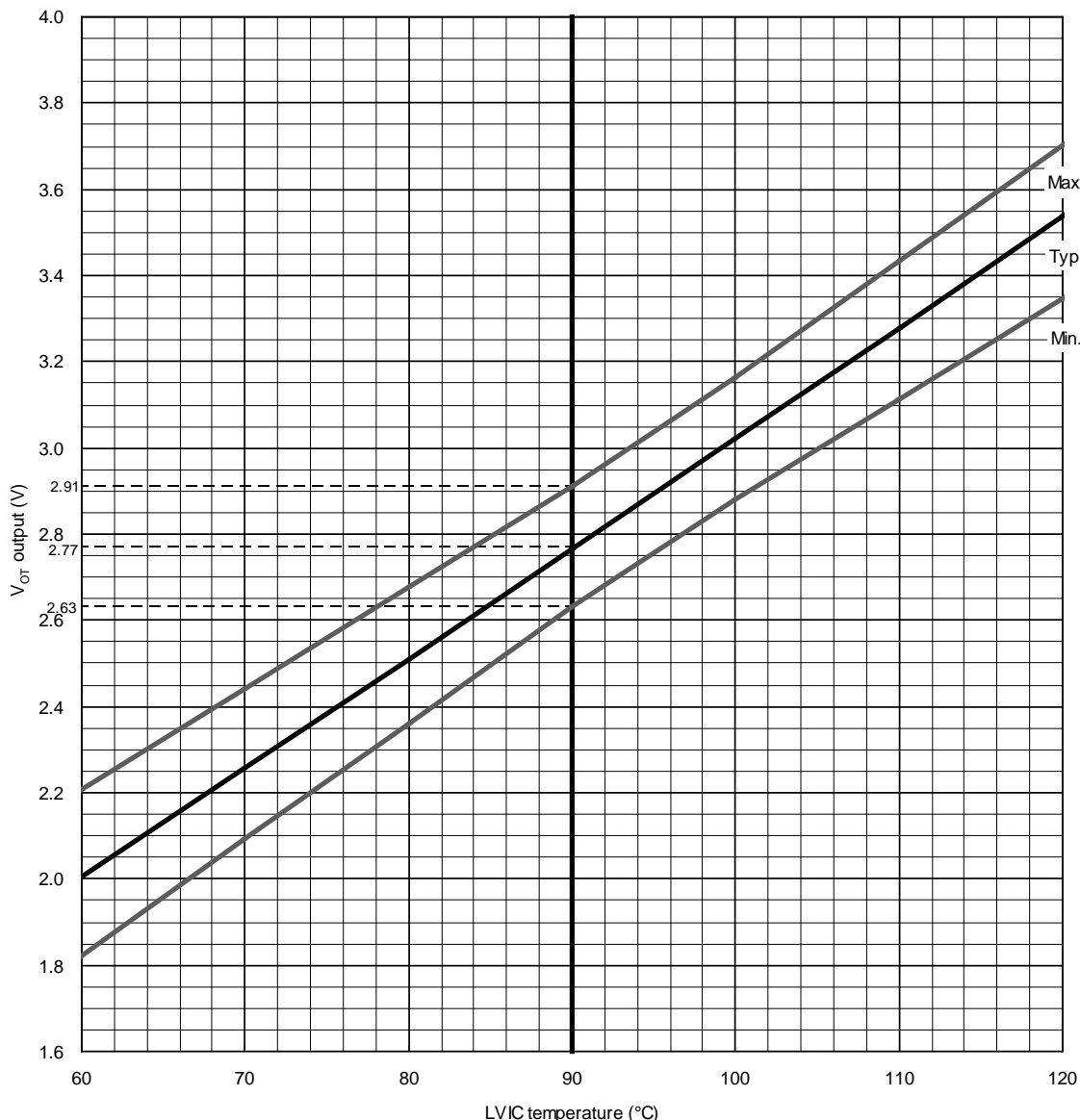
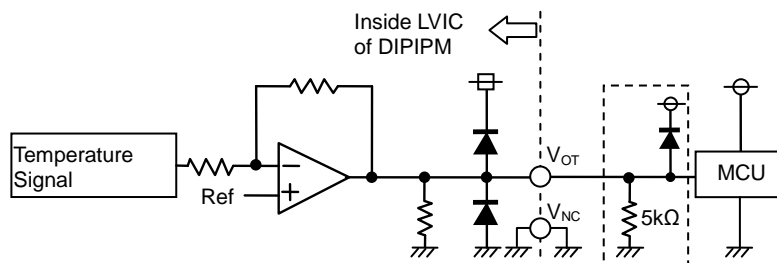


Fig. 4 V_{OT} output circuit



- (1) It is recommended to insert 5kΩ (5.1kΩ is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V_{OT} and V_{NC} (control GND), the extra circuit current, which is calculated approximately by V_{OT} output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V_{OT} for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
- (2) In the case of using V_{OT} with low voltage controller like 3.3V MCU, V_{OT} output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp Di between control supply of the controller and V_{OT} output for preventing over voltage destruction.
- (3) In the case of not using V_{OT} , leave V_{OT} output NC (No Connection).

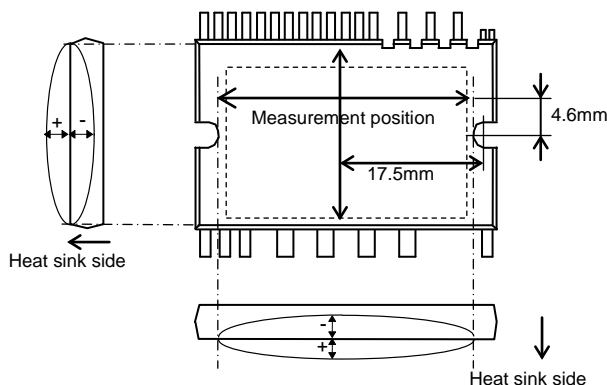
Refer the application note for this series about the usage of V_{OT} .

< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
 TRANSFER MOLDING TYPE
 INSULATED TYPE

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 9)	Recommended 0.69N·m	0.59	0.69	0.78	N·m
Terminal pulling strength	Control terminal: Load 4.9N Power terminal: Load 9.8N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Control terminal: Load 2.45N Power terminal: Load 4.9N 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	8.5	-	g
Heat-sink flatness	(Note 10)		-50	-	100	μm

Note 9: Plain washers (ISO 7089-7094) are recommended.
 Note 10: Measurement point of heat sink flatness

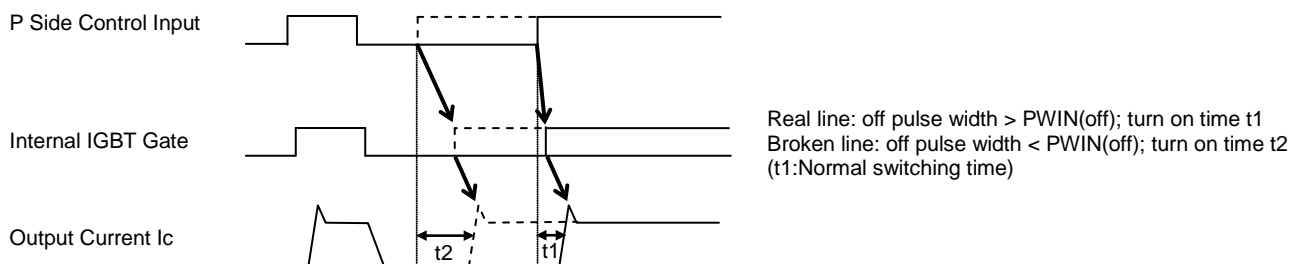


RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
V_D	Control supply voltage	Applied between $V_{P1}-V_{NC}$, $V_{N1}-V_{NC}$	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB-U} , V_{VFB-V} , V_{WFB-W}	13.0	15.0	18.5	V
$\Delta V_D, \Delta V_{DB}$	Control supply variation		-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal	2.0	-	-	μs
f_{PWM}	PWM input frequency	$T_C \leq 100^\circ C$, $T_j \leq 125^\circ C$	-	-	20	kHz
I_o	Allowable r.m.s. current	$V_{CC} = 300V$, $V_D = 15V$, P.F = 0.8, Sinusoidal PWM $T_C \leq 100^\circ C$, $T_j \leq 125^\circ C$ (Note11)	$f_{PWM} = 5kHz$	-	15.0	Arms
			$f_{PWM} = 15kHz$	-	10.0	
PWIN(on)		(Note 12)	0.7	-	-	μs
PWIN(off)	Minimum input pulse width	$200V \leq V_{CC} \leq 350V$, $13.5V \leq V_D \leq 16.5V$, $13.0V \leq V_{DB} \leq 18.5V$, $-30^\circ C \leq T_C \leq 100^\circ C$, N-line wiring inductance less than 10nH (Note 13)	Below rated current	0.7	-	
			Between rated current and 1.7 times of rated current	1.5	-	
V_{NC}	V_{NC} variation	Between $V_{NC}-NU, NV, NW$ (including surge)	-5.0	-	+5.0	V
T_j	Junction temperature		-20	-	+125	°C

Note 11: Allowable r.m.s. current depends on the actual application conditions.
 12: DIPIPM might not make response if the input signal pulse width is less than PWIN(off).
 13: IPM might make delayed response or no response for the input signal with off pulse width less than PWIN(off). Please refer below about delayed response.

Delayed Response against Shorter Input Off Signal than PWIN(off) (P-side only)

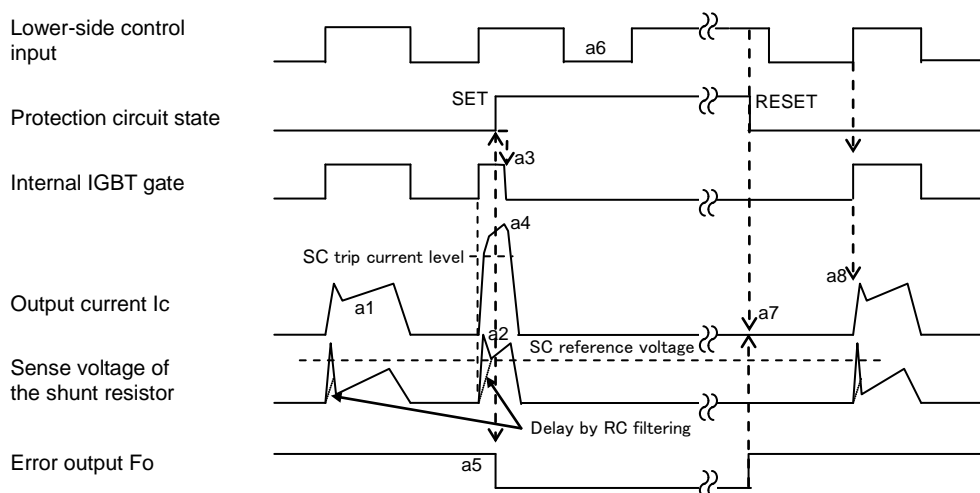


< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
 TRANSFER MOLDING TYPE
 INSULATED TYPE

Fig. 5 Timing Charts of The DIPIPM Protective Functions

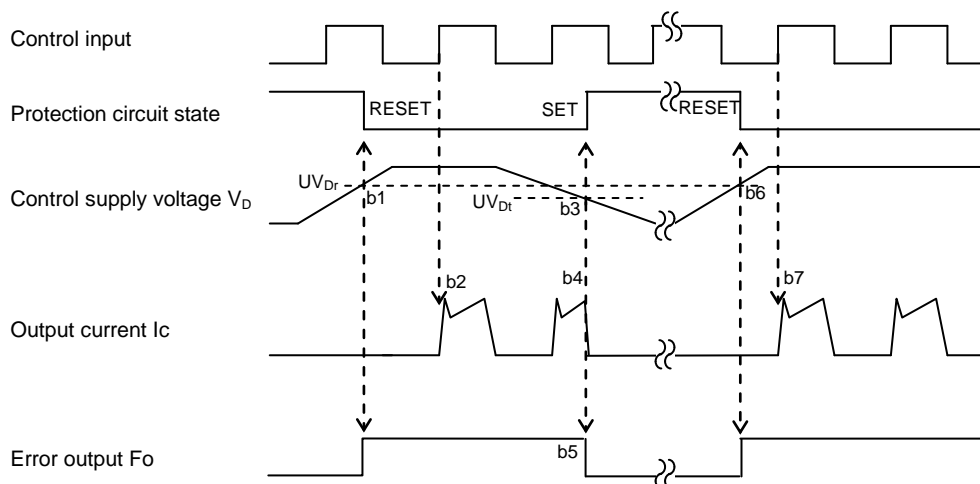
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger)
 (It is recommended to set RC time constant 1.5~2.0 μ s so that IGBT shut down within 2.0 μ s when SC.)
- a3. All N-side IGBT's gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. F_O outputs for t_{Fo}=minimum 20 μ s.
- a6. Input = "L": IGBT OFF
- a7. F_o finishes output, but IGBTs don't turn on until inputting next ON signal (L→H).
 (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.



[B] Under-Voltage Protection (N-side, UV_D)

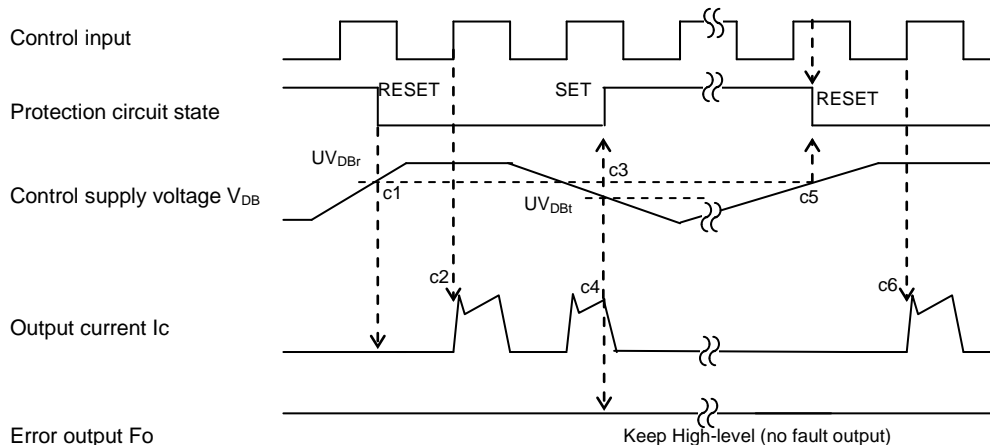
- b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but IGBT turns ON by next ON signal (L→H).
 (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: IGBT ON and outputs current.
- b3. V_D level drops to under voltage trip level. (UV_{Dt}).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5. F_o outputs for t_{Fo}=minimum 20 μ s, but output is extended during V_D keeps below UV_{Dr}.
- b6. V_D level reaches UV_{Dr}.
- b7. Normal operation: IGBT ON and outputs current.



< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
 TRANSFER MOLDING TYPE
 INSULATED TYPE

[C] Under-Voltage Protection (P-side, UV_{DB})

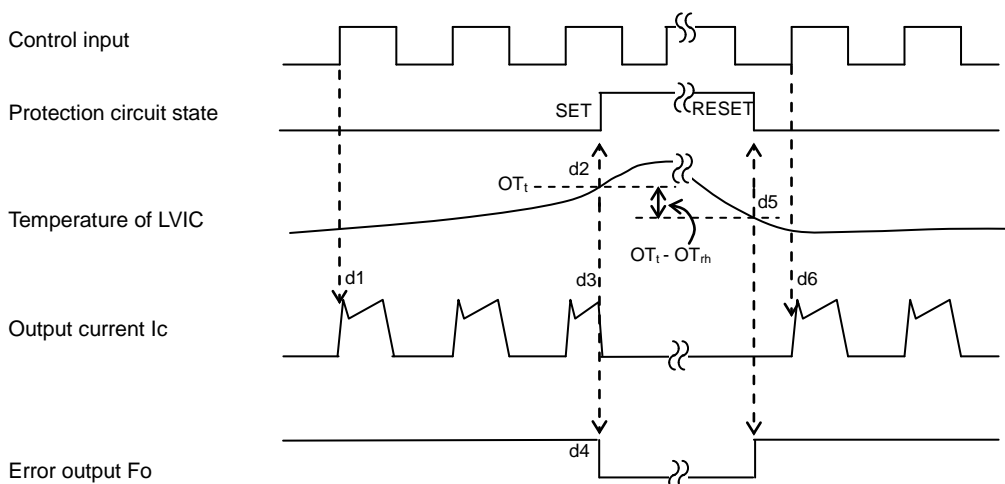
- c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr} , IGBT turns on by next ON signal (L→H).
- c2. Normal operation: IGBT ON and outputs current.
- c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
- c4. IGBT of the correspond phase only turns OFF in spite of control input signal level, but there is no F_o signal output.
- c5. V_{DB} level reaches UV_{DBr} .
- c6. Normal operation: IGBT ON and outputs current.



[D] Over Temperature Protection (N-side, Detecting LVIC temperature)

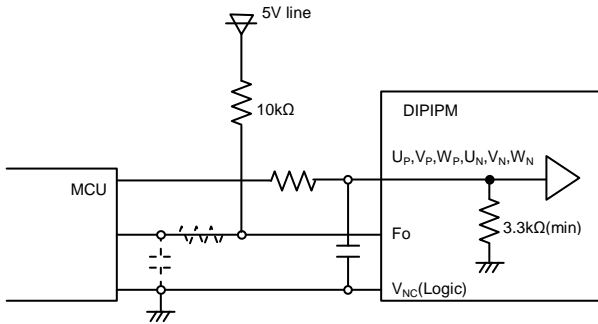
- d1. Normal operation: IGBT ON and outputs current.
- d2. LVIC temperature exceeds over temperature trip level (OT_t).
- d3. All N-side IGBTs turn OFF in spite of control input condition.
- d4. F_o outputs for t_{Fo} =minimum 20 μ s, but output is extended during LVIC temperature keeps over OT_t .
- d5. LVIC temperature drops to over temperature reset level.
- d6. Normal operation: IGBT turns on by next ON signal (L→H).

(IGBT of each phase can return to normal state by inputting ON signal to each phase.)



< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
 TRANSFER MOLDING TYPE
 INSULATED TYPE

Fig. 7 MCU I/O Interface Circuit



Note)

Design for input RC filter depends on PWM control scheme used in the application and wiring impedance of the printed circuit board. DIPIPM input signal interface integrates a minimum 3.3kΩ pull-down resistor. Therefore, when inserting RC filter, it is necessary to satisfy turn-on threshold voltage requirement. F_O output is open drain type. It should be pulled up to control power supply (e.g. 5V, 15V) with a resistor that makes F_O sink current I_{F_O} 1mA or less. In the case of pulled up to 5V supply, 10kΩ (5kΩ or more) is recommended.

Fig. 8 Pattern Wiring Around the Shunt Resistor

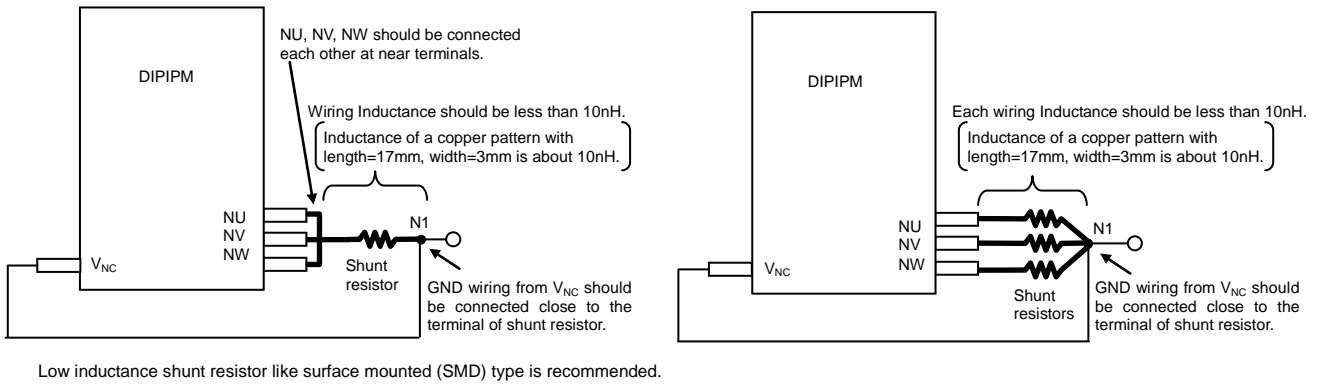
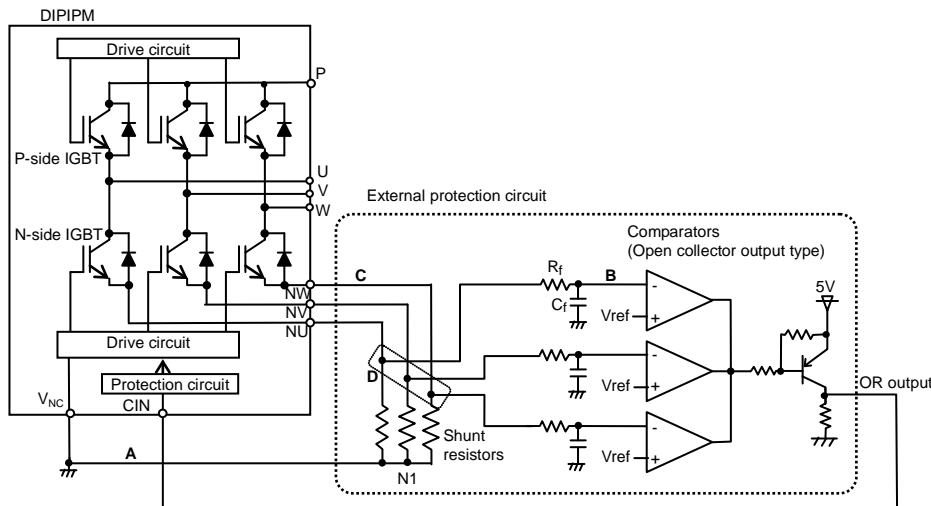


Fig. 9 Pattern Wiring Around the Shunt Resistor (for the case of open emitter)

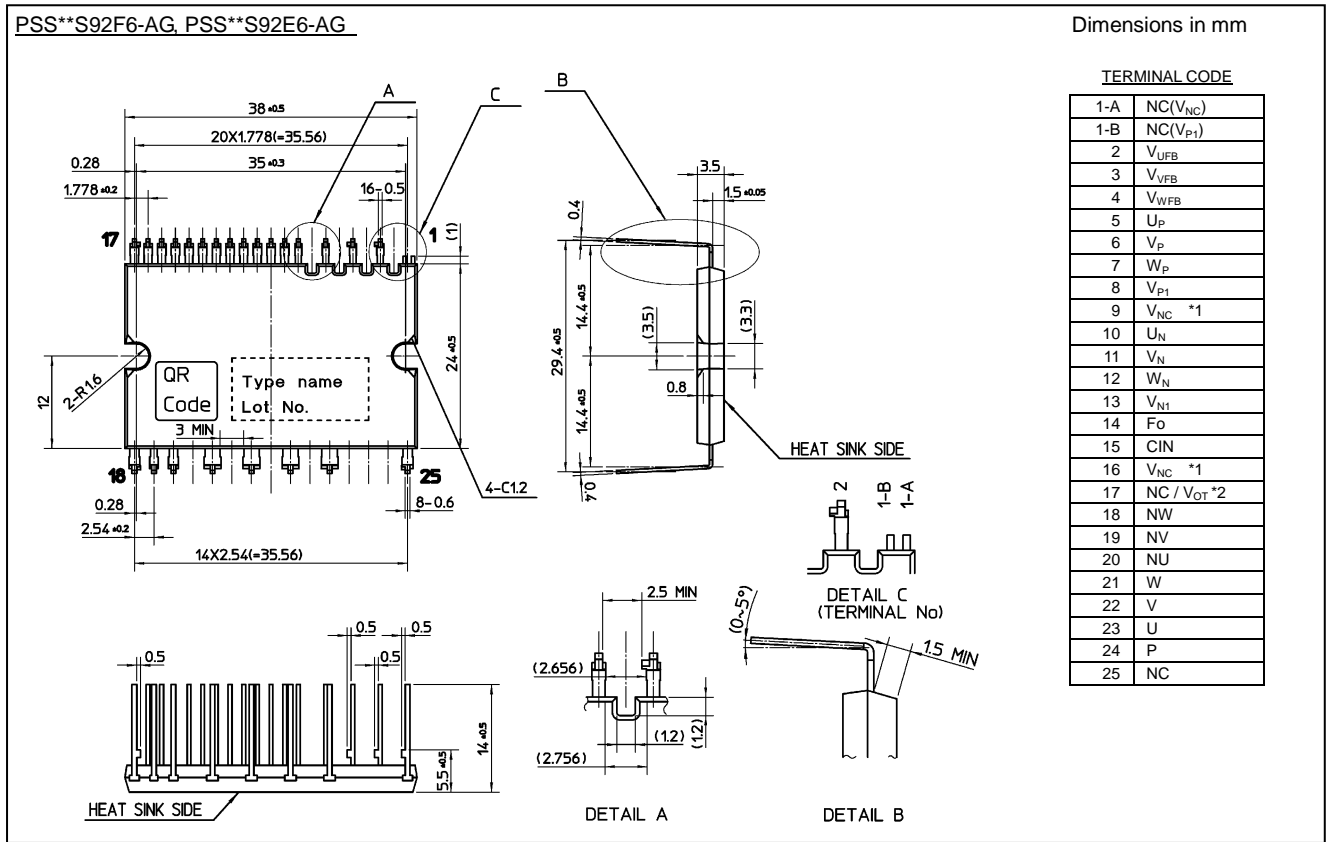
When DIPIPM is operated with three shunt resistors, voltage of each shunt resistor cannot be input to CIN terminal directly. In that case, it is necessary to use the external protection circuit as below.



- (1) It is necessary to set the time constant $R_f C_f$ of external comparator input so that IGBT stops within $2\mu s$ when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) It is recommended for the threshold voltage V_{ref} to set to the same rating of short circuit trip level ($V_{sc(ref)}$: typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified value (=1.7 times of rating current).
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be close to the terminal of shunt resistor.
- (6) OR output high level when protection works should be over 0.505V (=maximum $V_{sc(ref)}$ rating).

< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
 TRANSFER MOLDING TYPE
 INSULATED TYPE

Fig. 10 Package Outlines



- 1) 9 & 16 pins (V_{NC}) are connected inside DIPIPM, please connect either one to the control power supply GND outside and leave another one open.
- 2) No.17 is V_{OT} for built-in temperature output function type (PSS**S92F6-AG) and NC (No Connection) for built-in OT protection function type (PSS**S92E6-AG).

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< Dual-In-Line Package Intelligent Power Module >
PSS30S92F6-AG, PSS30S92E6-AG
TRANSFER MOLDING TYPE
INSULATED TYPE

Revision Record

Rev.	Date	Page	Revised contents
1	25/12/2013	-	New
2	15/03/2014	2	Add Note 1
		5	Revise misdescription about the condition of PWIN(off)

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